

The Embedded I/O Company



TAMC900-A1

Signal Conditioning Adapter for TAMC900

Version 1.0

User Manual

Issue 1.0.1

February 2010

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TAMC900-A1-10R

Signal Conditioning Adapter for TAMC900,
Gain = 1, RoHS compliant

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	Initial Issue	April 2008
1.0.1	- New Issue notation - General Revision	February 2010

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1 Product Description

The TAMC900-A1 is a simple Signal Conditioning Adapter (SiCA) providing I/O-connectors for the analog inputs, clock and trigger inputs and the analog signal conditioning.

All inputs are differential. The signal conditioning consists of a differential amplifier with gain=1 and a low pass filter to suppress high frequency noise.

The TAMC900-A1 provides eight analog, three clock and three trigger inputs.

For First-Time-Buyers the engineering documentation TAMC900-A1-ED is recommended. The engineering documentation includes TAMC900-A1-DOC, schematics and data sheets of TAMC900-A1.

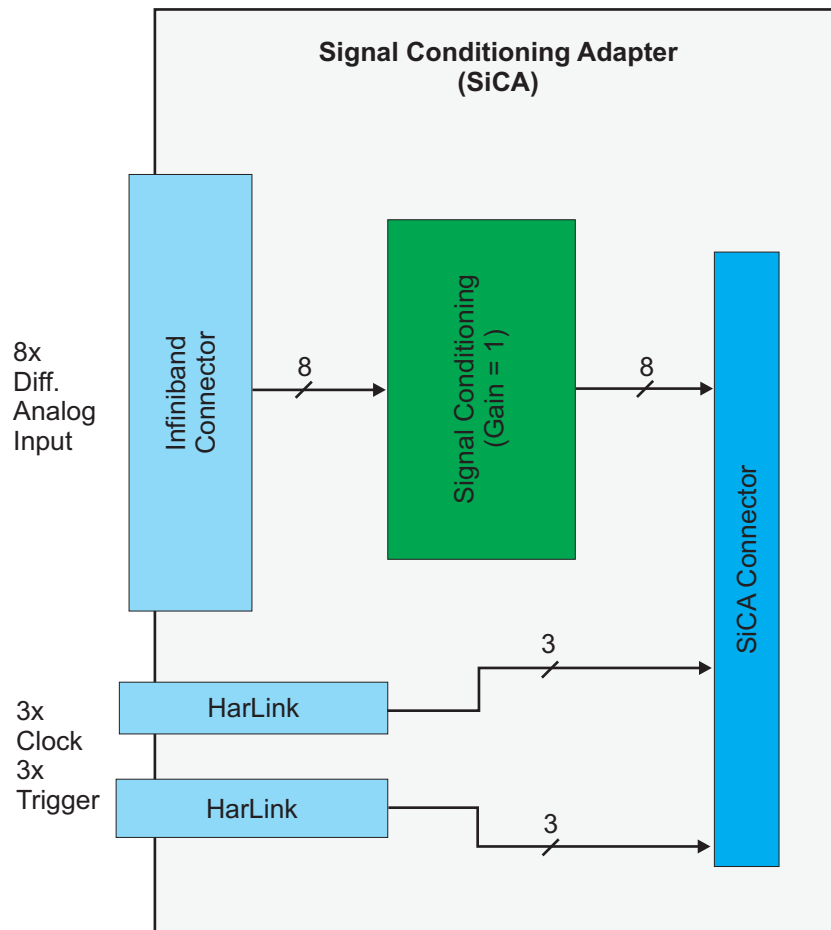


Figure 1-1 : Block Diagram TAMC900-A1

2 Technical Specification

AMC Interface	
Mechanical Interface	Signal Conditioning Adapter for TAMC900
Electrical Interface	compliant to TAMC900
I/O Interface	
Number of Analog Channels	8 differential via Infiniband Connector
Number of Clock Inputs	3 differential (LVDS) via HarLink Connector
Number of Trigger Inputs	3 differential (LVDS) via HarLink Connector
Analog Signal Conditioning	
Input Type	Differential
Input Voltage Range (diff.)	±1 Volt
Input Common Mode Voltage	0 – 3.3 Volt
Max. Differential Input Voltage	1.4 Volt
Gain	1
-3dB Bandwidth	0 – 67 MHz
Output Slew Rate	630 V/μs
Output Settling Time	11 ns (2 Volt Step, 0.1% Settling)
Output Common Mode Voltage	1.37 Volt
Physical Data	
Power Requirements	180 mA typical @ +6V DC
Temperature Range	Operating 0 °C to +55 °C Storage 0 °C to +70 °C
MTBF	804000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G _B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	50 g

Table 2-1 : Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection



The TAMC900-A1 is sensitive to static electricity. Packing, unpacking and all other handling of the TAMC900-A1 has to be done in an ESD/EOS protected area.

3.2 Maximum Input Voltage



The maximum input voltage of the Clock and Trigger inputs is 2.5 Volt. The TAMC900 will be damaged if higher voltage levels are used.



The allowed Common Mode Input Voltage range for the Analog Inputs is 0 – 3.3 Volt.

4 Analog Inputs

The TAMC900-A1 provides access to the analog inputs of the eight ADCs of the TAMC900. As signal conditioning, it provides a differential amplifier with Gain = 1 for each analog input.

The figure below shows one analog input path of the TAMC900-A1.

ANALOG_INx+ and ANALOG_INx- build one analog input of the TAMC900-A1, and the resistors R_I and R_F set the gain of the signal conditioning (gain = 1).

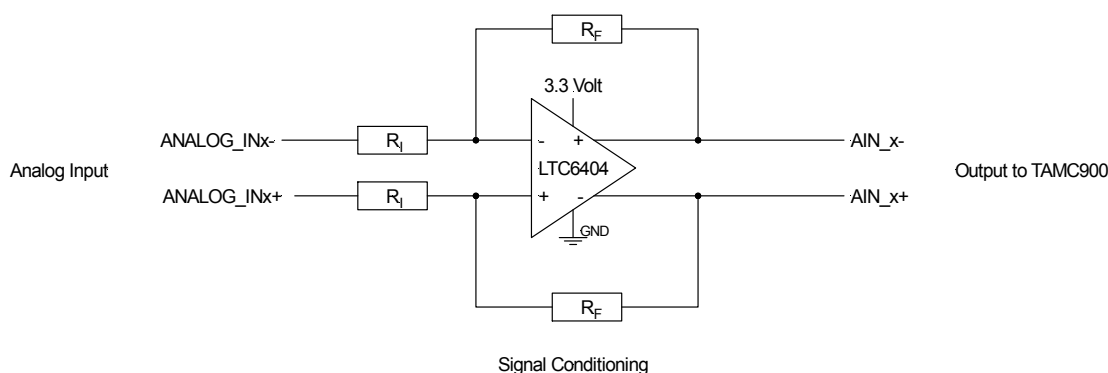


Figure 4-1 : Analog Input Block Diagram

An Infiniband connector (FCI 58368-111010 or compatible) is used for the analog inputs.



A differential signal is composed of two (ground referenced) single ended signals.
For each analog input, you need to connect three signals:
ANALOG_IN+, ANALOG_IN-, and GND

4.1 Input Voltage Range

The common mode voltage range of the analog inputs is 0 – 3.3 Volt, and independent from the output common mode voltage.

The maximum differential input voltage V_{INDIFF} (difference between ANALOG_INx+ and ANALOG_INx-) should be limited to ± 1.0 Volt, because this is the input range of the ADCs on the TAMC900.

Please refer to the LTC6406 data sheet for more details. The data sheet is part of the Engineering documentation.



For optimal performance, do not exceed the maximum differential input voltage range of the TAMC900 ADCs.

4.2 Single Ended Signal Source

If a single ended signal source is used, it can be connected to the TAMC900-A1 in the following way:

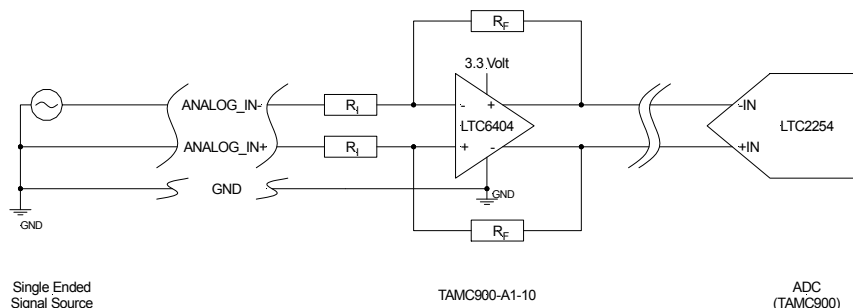


Figure 4-2 : Single Ended Signal Source

In the above configuration, ANALOG_IN- should not exceed ± 1.0 Volt (ADC input voltage range).

Unfortunately, most signal sources have a non-zero output impedance R_S . This causes feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the input source output impedance be compensated for. If input impedance matching is required by the source, a termination resistor R_T should be chosen:

$$R_T = \frac{200\Omega \times R_S}{200\Omega - R_S} \quad (200\ \Omega \text{ is the input impedance of ANALOG_IN-})$$

To provide differential balance, R_{DB} is chosen to equal $R_T \parallel R_S$:

$$R_{DB} = \frac{R_T R_S}{R_T + R_S}$$

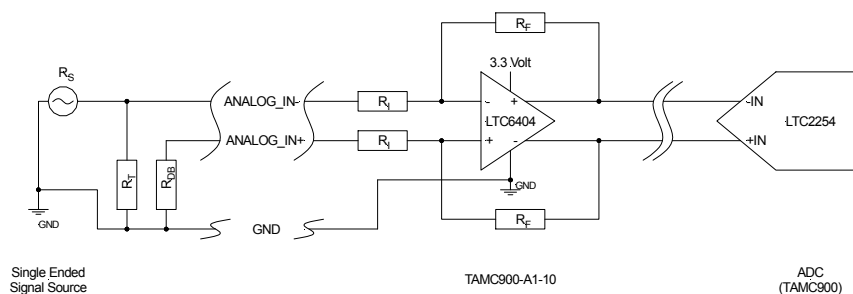


Figure 4-3 : Single Ended Signal Source with impedance matching

The overall single-ended to differential gain ($GAIN_{SE}$) must take into account the input attenuation of the R_S and R_T resistive divider and the effect of adding R_{DB} :

$$GAIN_{SE} = \frac{(300 + R_{DB})(150(R_S - R_T) + R_S R_T)}{R_S R_T (150 + R_{DB})}$$

5 Clock

All three differential clock inputs are directly routed to the SiCA Connector.

A Harting connector 27 21 121 8000 or compatible is used for the Clock inputs.



**The Clock Inputs are directly routed to the TAMC900.
The maximum input voltage of the corresponding Virtex-5 I/Os is 2.5 Volt.
The device will be damaged if higher voltage levels are used.**

6 Trigger

All three differential Trigger inputs are directly routed to the SiCA connector.

A Harting connector 27 21 121 8000 or compatible is used for the Trigger inputs.



**The Trigger Inputs are directly routed to the TAMC900.
The maximum input voltage of the corresponding Virtex-5 I/Os is 2.5 Volt.
The device will be damaged if higher voltage levels are used.**

7 Pin Assignment

7.1 Overview

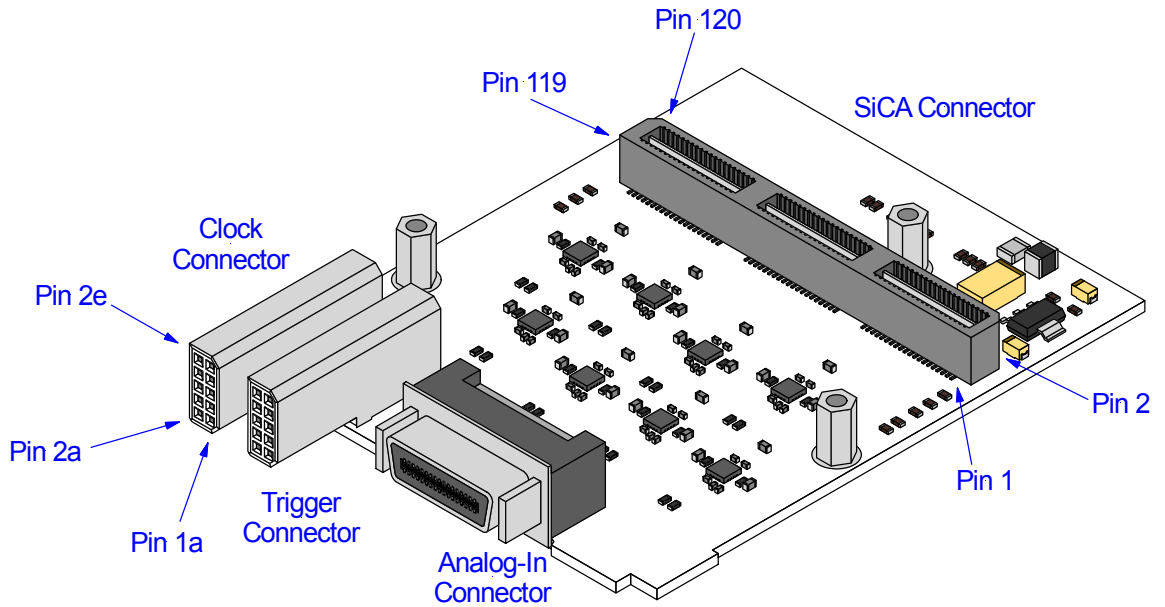


Figure 7-1 : Connector Overview

7.2 Clock Connector

Pin	Signal	Level
1a	CLKIN_2+	LVDS
1b	GND	
1c	CLKIN_1+	LVDS
1d	GND	
1e	CLKIN_0+	LVDS
1z	CASE	Front Panel

Pin	Signal	Level
2a	CLKIN_2-	LVDS
2b	GND	
2c	CLKIN_1-	LVDS
2d	GND	
2e	CLKIN_0-	LVDS
2z	CASE	Front panel

Table 7-1 : Pin Assignment Clock Connector

7.3 Trigger Connector

Pin	Signal	Level
1a	TRIG_2+	LVDS
1b	GND	
1c	TRIG_1+	LVDS
1d	GND	
1e	TRIG_0+	LVDS
1z	CASE	Front Panel

Pin	Signal	Level
2a	TRIG_2-	LVDS
2b	GND	
2c	TRIG_1-	LVDS
2d	GND	
2e	TRIG_0-	LVDS
2z	CASE	Front panel

Table 7-2 : Pin Assignment Trigger Connector

7.4 Analog-In Connector

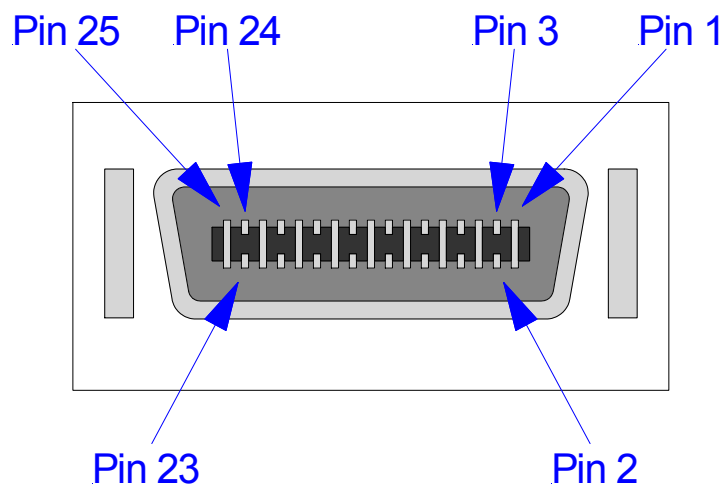


Figure 7-2 : Pin Locations Analog-In Connector

Pin	Signal	Level
1	GND	
2	ANALOG_IN0-	0 – 3.3 Volt
4	GND	
5	ANALOG_IN1-	0 – 3.3 Volt
7	GND	
8	ANALOG_IN2-	0 – 3.3 Volt
10	GND	
11	ANALOG_IN3-	0 – 3.3 Volt
13	GND	

Pin	Signal	Level
3	ANALOG_IN0+	0 – 3.3 Volt
6	ANALOG_IN1+	0 – 3.3 Volt
9	ANALOG_IN2+	0 – 3.3 Volt
12	ANALOG_IN3+	0 – 3.3 Volt

Pin	Signal	Level
14	ANALOG_IN4-	0 – 3.3 Volt
16	GND	
17	ANALOG_IN5-	0 – 3.3 Volt
19	GND	
20	ANALOG_IN6-	0 – 3.3 Volt
22	GND	
23	ANALOG_IN7-	0 – 3.3 Volt
25	GND	

Pin	Signal	Level
15	ANALOG_IN4+	0 – 3.3 Volt
18	ANALOG_IN5+	0 – 3.3 Volt
21	ANALOG_IN6+	0 – 3.3 Volt
24	ANALOG_IN7+	0 – 3.3 Volt

Table 7-3 : Pin Assignment Analog-In Connector

7.5 SiCA Connector

The Samtec QTE / QSE Series are used as I/O connection between TAMC900 and the SiCA. The TAMC900 carries a QSE connector, and the mating QTE connector is populated on the SiCA. The stacking height is defined by the QTE connector on the SiCA.

The Samtec QTE-060-02-L-D-A or compatible is used on the TAMC900-A1.

Pin	Signal	Level
1	GP_IO_0	2,5 Volt CMOS
3	GP_IO_1	2,5 Volt CMOS
5	GP_IO_2	2,5 Volt CMOS
7	GP_IO_3	2,5 Volt CMOS
9	GP_IO_4	2,5 Volt CMOS
11	GP_IO_5	2,5 Volt CMOS
13	GP_IO_6	2,5 Volt CMOS
15	GP_IO_7	2,5 Volt CMOS
17	GP_IO_8	2,5 Volt CMOS
19	GP_IO_9	2,5 Volt CMOS
21	GND	logic Ground
23	-	-
25	-	-
27	-	-
29	-	-
31	GND	logic Ground
33	GND	logic Ground
35	AIN_0-	0 – 2.9 Volt
37	AIN_0+	
39	GND	logic Ground

Pin	Signal	Level
2	SiCA_PWR	+6 Volt
4	SiCA_PWR	+6 Volt
6	SiCA_PWR	+6 Volt
8	SiCA_PWR	+6 Volt
10	SiCA_PWR	+6 Volt
12	SiCA_PWR	+6 Volt
14	GND	logic Ground
16	GND	logic Ground
18	LVDS_0+	LVDS
20	LVDS_0-	LVDS
22	GND	logic Ground
24	LVDS_1+	LVDS
26	LVDS_1-	LVDS
28	GND	logic Ground
30	LVDS_2+	LVDS
32	LVDS_2-	LVDS
34	GND	logic Ground
36	LVDS_3+	LVDS
38	LVDS_3-	LVDS
40	GND	logic Ground

Pin	Signal	Level
41	GND	logic Ground
43	AIN_1-	0 – 2.9 Volt
45	AIN_1+	
47	GND	logic Ground
49	GND	logic Ground
51	AIN_2-	0 – 2.9 Volt
53	AIN_2+	
55	GND	logic Ground
57	GND	logic Ground
59	AIN_3-	0 – 2.9 Volt
61	AIN_3+	
63	GND	logic Ground
65	GND	logic Ground
67	AIN_4-	0 – 2.9 Volt
69	AIN_4+	
71	GND	logic Ground
73	GND	logic Ground
75	AIN_5-	0 – 2.9 Volt
77	AIN_5+	
79	GND	logic Ground
81	GND	logic Ground
83	AIN_6-	0 – 2.9 Volt
85	AIN_6+	
87	GND	logic Ground
89	GND	logic Ground
91	AIN_7-	0 – 2.9 Volt
93	AIN_7+	
95	GND	logic Ground
97	GND	logic Ground
99	-	-
101	-	-
103	-	-
105	-	-
107	GND	logic Ground
109	GP_IO_10	2,5 Volt CMOS
111	GP_IO_11	2,5 Volt CMOS

Pin	Signal	Level
42	GND	logic Ground
44	LVDS_4+	LVDS
46	LVDS_4-	LVDS
48	GND	logic Ground
50	LVDS_5+	LVDS
52	LVDS_5-	LVDS
54	GND	logic Ground
56	LVDS_6+	LVDS
58	LVDS_6-	LVDS
60	GND	logic Ground
62	LVDS_7+	LVDS
64	LVDS_7-	LVDS
66	GND	logic Ground
68	LVDS_8+	LVDS
70	LVDS_8-	LVDS
72	GND	logic Ground
74	LVDS_9+	LVDS
76	LVDS_9-	LVDS
78	GND	logic Ground
80	GND	logic Ground
82	GND	logic Ground
84	TRIG_0+	LVDS
86	TRIG_0-	LVDS
88	GND	logic Ground
90	TRIG_1+	LVDS
92	TRIG_1-	LVDS
94	GND	logic Ground
96	TRIG_2+	LVDS
98	TRIG_2-	LVDS
100	GND	logic Ground
102	GND	logic Ground
104	CLKIN_0+	LVDS
106	CLKIN_0-	LVDS
108	GND	logic Ground
110	CLKIN_1+	LVDS
112	CLKIN_1-	LVDS

Pin	Signal	Level
113	GP_IO_12	2,5 Volt CMOS
115	GP_IO_13	2,5 Volt CMOS
117	GP_IO_14	2,5 Volt CMOS
119	GP_IO_15	2,5 Volt CMOS

Pin	Signal	Level
114	GND	logic Ground
116	CLKIN_2+	LVDS
118	CLKIN_2-	LVDS
120	GND	logic Ground

Table 7-4 : Pin Assignment SiCA Connector