The Embedded I/O Company

TEWS TECHNOLOGIES

TCP631

Reconfigurable FPGA

Version 1.0

User Manual

Issue 1.0.3

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TPMC631-10

Reconfigurable FPGA, 1,500k Gates

TPMC631-11

Reconfigurable FPGA, 5,000k Gates

TPMC631-20

Reconfigurable FPGA, 1,500k Gates, J2 Rear I/O

TPMC631-21

Reconfigurable FPGA, 5,000k Gates, J2 Rear I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
0.0.1	Preliminary Issue	April 2009
1.0.0	Initial Issue	June 2009
1.0.1	Added master example	July 2009
1.0.2	Elaborated “6.2 Configuration File Creation“ and added “6.2.1.1 Using the iMPACT GUI” Added “7.1 FPGA Bank Usage” Added design warning “7.4.1 Designs Intended for FPGA JTAG Configuration”	April 2010
1.0.3	Clarified PCI-to-local space mapping in the Appendix section	September 2010

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1 Product Description

The TCP631 is a standard 3U 32 bit CompactPCI module providing a user configurable FPGA with 1,500,000 or 5,000,000 system gates. All local signals from the PCI controller are routed to the FPGA.

The TCP631 offers 64 I/O lines to the front I/O and 64 I/O lines to the rear I/O. For flexible front I/O solutions the TCP631 provides a PIM Module slot, allowing active and passive signal conditioning. An option offers additionally 64 I/O lines via the J2 connector. All I/O lines are directly connected to the FPGA-pins, which maintains the flexibility of the Select I/O technology of the Spartan III FPGA. All I/O lines provide external ESD-protection devices. In addition the FPGA is connected to two banks of 128 Mbytes, 16 bit wide DDR2 SDRAM.

The FPGA is configured by a parallel flash. The flash device is in-system programmable via driver software over the PCI bus. An in-circuit debugging option is available via an optionally mountable JTAG header for readback and real-time debugging of the FPGA design (using Xilinx “ChipScope”).

A programmable clock generator supplies up to four different clock frequencies between 5 kHz and 200 MHz which are available at the FPGA, in addition one clock source is used as the local clock signal for the PCI controller. The clock generator settings are stored in an EEPROM and can be changed by the driver software.

The configuration EEPROM of the PCI controller can also be modified by the driver software, to adapt address spaces etc.

User applications for the TCP631-x0 can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com. User applications for the TCP631-x1 require the full ISE Foundation software, which must be purchased from Xilinx.

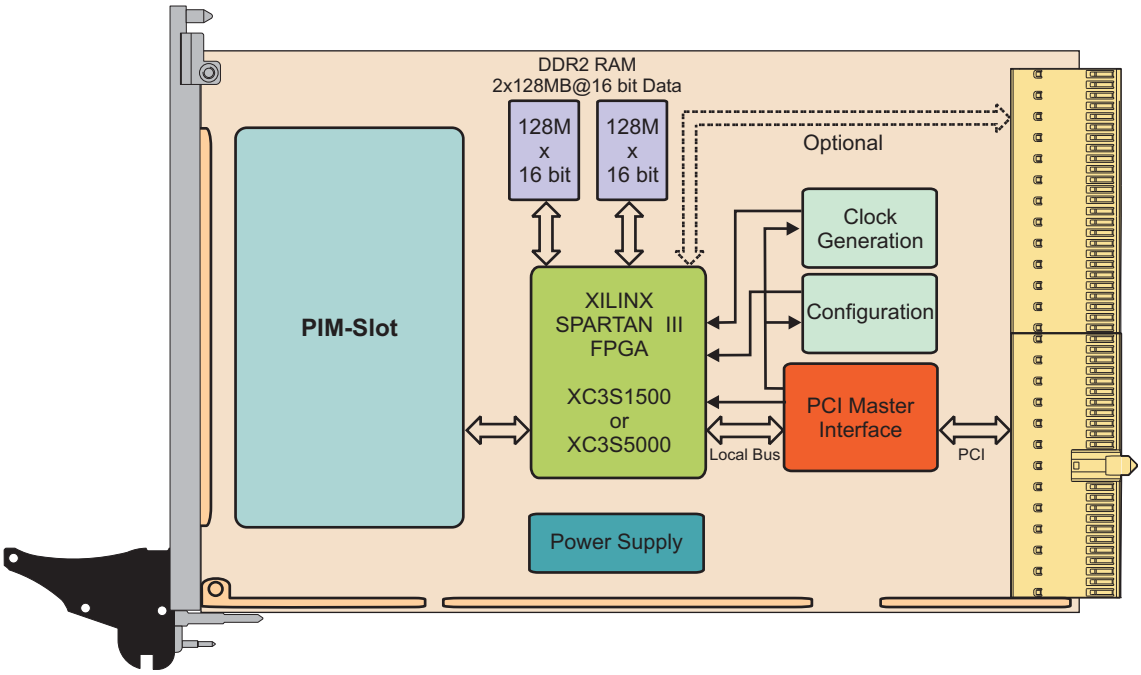

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	Standard 3U 32 Bit CompactPCI module conforming to PICMG 2.0 R3.0	
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9056 (PLX Technology)	
User configurable FPGA	TCP631-x0: XC3S1500-4 (Xilinx) TCP631-x1: XC3S5000-4 (Xilinx)	
DDR2 RAM	MT47H64M16 (Micron) 64 Meg x 16 Bit	
Programmable Clock Generator	5V9885 (IDT)	
I/O Interface		
Number of Channels	PIM Slot I/O: 64x 3.3V LVTTL I/O J2 I/O: 64x 3.3V LVTTL I/O	
I/O Connector	The TCP631 provides 64 I/O lines to a PIM slot instead of a front I/O connector TCP631-2x: provides additional 64 I/O lines to the 110 pol. CompactPCI back I/O (J2)	
Physical Data		
Power Requirements	Depends on FPGA design. 700 mA typical @ +3.3V DC (DDR2 Example design) Additional power is used by the PIM.	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	480 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	146 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instruction

3.1 ESD Protection

The TCP631 is sensitive to static electricity. Packing, unpacking and all other handling of the TCP631 has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

The TCP631 requires forced air cooling during operation. Without forced air cooling, damage to the device can occur.

3.3 I/O Signaling Voltages

The 64 FPGA I/O-Lines to the PIM Slot and the 64 FPGA I/O-Lines to J2 Rear I/O are connected to unbuffered FPGA I/O pins. The I/O voltage of these FPGA I/O pins is 3.3V maximum.

The FPGA I/O pins are NOT 5V tolerant.

4 PCI9056 Target Chip

The TCP631 uses the PLX PCI9056 32 bit, 66 MHz PCI bus mastering I/O accelerator as PCI-to-Local bus bridge. As default the PCI9056 is configured as PCI target, but it can also be used as PCI master with DMA capabilities.

The PCI9056 local bus type is the “C Mode” with non-multiplexed address and data lines.

4.1 PCI9056 Header

PCI CFG Register Address	Write ‘0’ to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	2277 1498
0x04	Status				Command				Y	0280 0000
0x08	Class Code						Revision ID		N	118000 BA
0x0C	BIST		Header Type		PCI Latency Timer		Cache Line Size		Y	00 00 00 00
0x10	PCI Base Address for MEM Mapped Config. Registers (PCIBAR0)								Y	FFFFFE00
0x14	PCI Base Address for IO Mapped Config. Registers (PCIBAR1)								Y	00000001
0x18	PCI Base Address for Local Address Space 0 (PCIBAR2)								Y	FFF00000
0x1C	PCI Base Address for Local Address Space 1 (PCIBAR3)								Y	FFF00000
0x20	Reserved								N	00000000
0x24	Reserved								N	00000000
0x28	PCI CardBus Information Structure Pointer								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	s.b. 1498
0x30	PCI Base Address for Local Expansion ROM								Y	00000000
0x34	Reserved						New Cap. Ptr.		N	000000 40
0x38	Reserved								N	00000000
0x3C	Max_Lat		Min_Gnt		Wire Interrupt		Interrupt Line		Y	00 00 01 00
0x40	PM Cap.				PM Nxt Cap.		PM Cap. ID		N	0002 48 01
0x44	PM Data		PM CSR EXT		PM CSR				Y	00 00 0000
0x48	Reserved		HS CSR		HS Nxt Cap.		HS Cap. ID		Y	00 00 4C 06
0x4C	VPD Address				VPD Nxt Cap.		VPD Cap. ID		Y	0000 00 03
0x50	VPD Data								Y	00000000

Table 4-1 : PCI Configuration Registers (PCR)

Subsystem-ID Value (Offset 0x2E): TCP631-10 0x200A

TCP631-11 0x200B

TCP631-20 0x2014

TCP631-21 0x2015

4.2 PCI9056 Address Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9056 address spaces PCIBAR0 – PCIBAR3.

PCI9056 Local Space	PCI9056 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Local Port Width (Bit)	Endian Mode	Description
-	0 (0x10)	MEM	512	-	-	PCIBAR0
-	1 (0x14)	I/O	256	-	-	PCIBAR1
0	2 (0x18)	MEM	1M	32	Little	PCIBAR2 Local Space 0
1	3 (0x1C)	MEM	1M	32	Little	PCIBAR3 Local Space 1
-	(0x30)	MEM	-	32	Little	Expansion ROM (Disabled)

Table 4-2 : PCI9056 Address Space Configuration

4.3 Default Configuration

With few exceptions the TCP631 default PCI9056 settings correspond to the PCI9056 “Values after Reset”. The exceptions, mainly the Local Address Space settings, are described here.

4.3.1 Local Address Spaces

The PCI9056 local bus type is the “C Mode” with non-multiplexed address and data lines.

PCI9056 Local Space	PCI Space Mapping	Size (Byte)	Base Address	Local Port Width (Bit)	Endian Mode	Description
0	MEM	1M	0x8000 0000	32	Little	No Wait States Ready Enabled Prefetch Disabled Burst Disabled
1	MEM	1M	0x0000 0000	32	Little	No Wait States Ready Enabled Prefetch Disabled Burst Disabled
Exp. ROM	MEM	-	-	32	Little	Expansion ROM (disabled)

Table 4-3 : Default Local Space Configuration

4.3.2 Other Settings

PCI9056 Register	Description	Value
LCS_PCIIDR	Device ID (TCP631) Vendor ID (TEWS Technologies)	0x2277 0x1498
LCS_PCICCR	Class Code (Other data acquisition/signal processing controllers)	0x118000
LCS_MARBR	PCI Compliance Enable	1
LCS_LMISC1	Local Init Status	1
LCS_PCISID	Subsystem Device ID (Build Option)	variable
LCS_PCISVID	Subsystem Vendor ID (TEWS Technologies)	0x1498

Table 4-4 : Other Default Configuration Settings

4.4 Configuration EEPROM

After power-on or PCI reset, the PCI9056 loads initial configuration register data from the on board configuration EEPROM. The TCP631 uses the “Extra Long Load Mode”, so the PCI9056 loads 50 16-bit words from the serial EEPROM.

Refer to the PCI9056 Manual for more information.

Yellow highlighted values can be modified by the driver software. From address 0x64 the EEPROM is free for user data, such as Vital Product Data (VPD). Access to the not highlighted values is prevented by the driver because these values are essential to driver function and board recognition.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x2277	0x1498	0x1180	0x00BA	0x0000	0x0100	0x0000	0x0000
0x10	0x0000	0x0000	0xFFF0	0x0000	0x8000	0x0001	0x0120	0x0000
0x20	0x0030	0x0500	0x0000	0x0000	0x0000	0x0000	0x4243	0x0243
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x40	0x0000	0x0000	s. b.	0x1498	0xFFF0	0x0000	0x0000	0x0001
0x50	0x0000	0x0243	0x0000	0x4C06	0x0000	0x0000	0x0002	0x4801
0x60	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x70	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x80	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-5 : Configuration EEPROM TCP631

Subsystem-ID Value (Offset 0x44):

TCP631-10	0x200A
TCP631-11	0x200B
TCP631-20	0x2014
TCP631-21	0x2015

4.5 Change of PCI9056 Settings

The TEWS driver software provides EEPROM read and write functions. If these are not used, refer to the PCI9056 manual how to access the EEPROM.

For details refer to the PCI9056 manual or the Configuration Register application note from PLX.

4.6 PCI9056 Interrupt enable

To use interrupts, bit 11 (Local Interrupt Input Enable) of the LCS_INTCSR (LCS Interrupt Control/Status, Local MEM BASE0 offset 0x068) must be set to “1”.

For further information please refer to the PCI9056 manual.

4.7 PCI9056 Master enable

The PCI9056 supports access to the PCI Bus from the local side. The Master mode must be enabled in the PCI Command register (PCICR[2]=1). This can also be accomplished from the local side.

For further information please refer to the PCI9056 manual.

5 Functional Description

5.1 PIM Module Slot

Instead of a front I/O Connector the TCP631 offers a PIM module slot. This allows a wide range of connectors to be used with the TCP631 and special I/O solutions can be easily applied with the TCP631.

The PIM standard is described in: “PMC I/O Module Standard (Vita 36)”, available at www.vita.com.

A PIM module is a 74 mm x 69 mm module with a PMC bezel and two EIA E700 AAAB connectors (as on PMCs). One of these connectors provides the power supply (3.3V, 5V & ±12V) for the PIM module, the other connector provides the I/O signals to the host board.

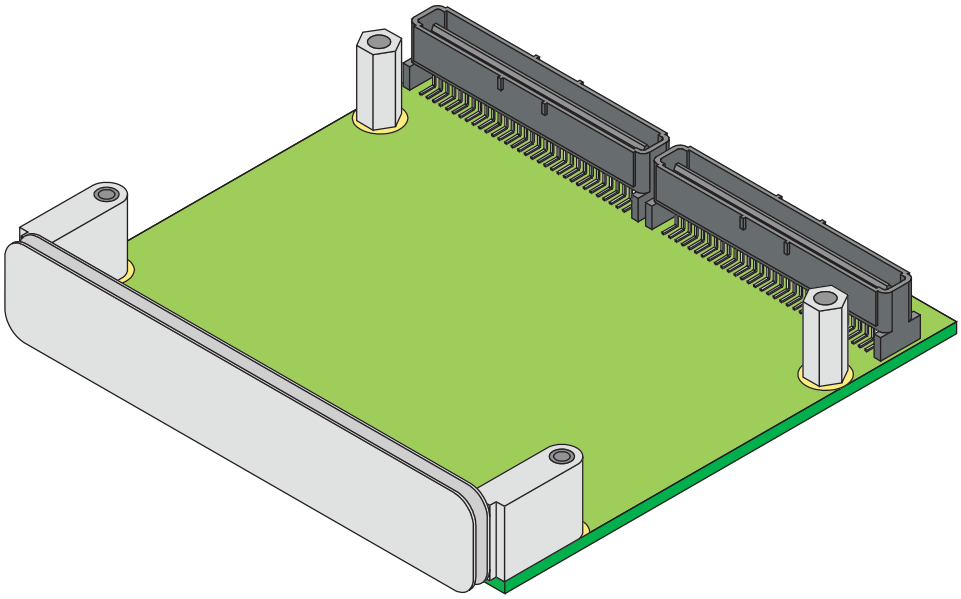

Figure 5-1 : A PIM Module

The PIM module can adapt the TCP631 to various I/O standards, either mechanical (connector) or electrical. A collection of PIM modules with standard I/O connectors are available from TEWS.

Example: A TPIM003 with an HD68 connector would offer all 64 FPGA I/O lines at the connector, with a pin assignment that is similar to a TCP630.

5.2 Electrical Interface

The 64 FPGA I/O-Lines to the PIM Slot and the 64 FPGA I/O-Lines to J2 Rear I/O are connected to unbuffered FPGA I/O pins. The I/O voltage of these FPGA I/O pins is 3.3V maximum.

The FPGA I/O pins are NOT 5V tolerant.

The following protection circuit is implemented on each I/O line:

- 33Ω Serial resistors
- Protection Devices (NZQA5V6A TVS-Array)

5.3 LEDs

Two “Circuit Board Indicators”, LED A and LED B, each with two FPGA controlled LEDs, are mounted in the front panel. The front panel LEDs are active low.

Indicator	Color	FPGA Pin	Position	Description
LED A	Red	F7	Front Panel	User controlled dual-LED, function depends on user application
	Green	F8		
LED B	Red	F15	Front Panel	User controlled dual-LED, function depends on user application
	Green	F16		

Table 5-1 : Front Panel LEDs

In addition an on board FPGA-DONE LED is provided.

Indicator	Color	FPGA Pin	Position	Description
DONE	Green	-	On Board	FPGA DONE-Pin LED (indicates successful FPGA configuration)

Table 5-2 : On Board LEDs

5.4 Clock Programming

IDT supplies the “IDT Programmable Clock” programming software, which can be used to change the clock settings. The input of the clock generator is the common 48 MHz local bus clock. The default clock settings are:

IDT Pin	Frequency	FPGA Pin	Description
REF IN	48MHz	AF14	Common local bus clock (CLK)
IDT Pin	**Frequency**	**FPGA Pin**	**Description**
OUT1	48MHz	AE14	Feed trough input clock (UCLK1)
OUT 2	133MHz	AE13	DDR2 RAM system clock (CLK_DDR)
OUT 3	14.7456MHz	C14	Clock for standard baud-rate generation (UCLK2)
OUT 4	40MHz	A13	Even numbered frequency (UCLK3)
OUT 5	-	-	Unused, not connected to the FPGA
OUT 6	-	-	Unused, not connected to the FPGA

Table 5-3 : Clock Programming

When changing the clock settings, following rule must be observed:

The clock generator device offers 4 configuration sets. These must be identical; otherwise the device will load invalid configuration data on power up.

5.5 Local Bus

The PCI9056 runs in the "C" local bus mode (Intel/Generic 32-bit address and data, non-multiplexed).

5.5.1 Local Bus Signals

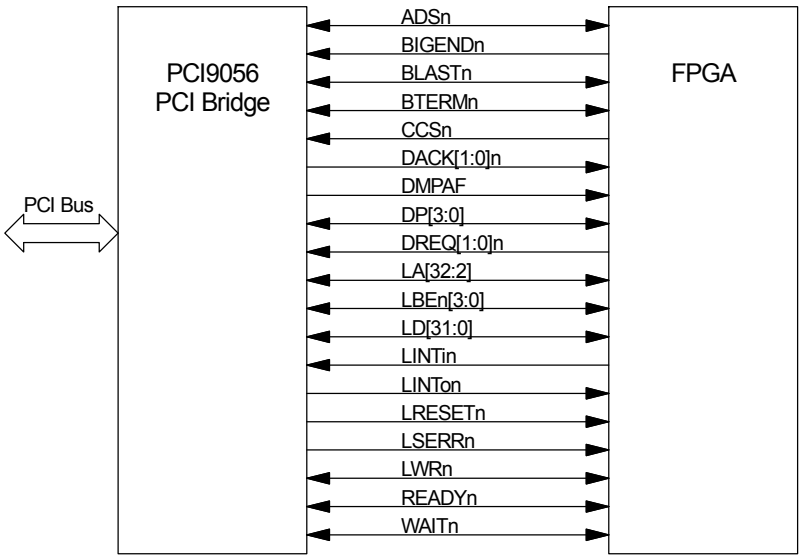

Figure 5-2 : Local Bus Signals

All PCI9056 local bus signals are connected to the FPGA. Some are optional or only needed in master capable designs. Refer to the PCI9056 Data Book for a detailed signal description.

Signal	Direction PCI9056 ←→ FPGA	Pull up	Description
ADSn	←→		Address Strobe
BIGENDn	←	yes	Big Endian Select
BLASTn	←→	yes	Burst Last
BTERMn	←→	yes	Burst Terminate
CCSn	←	yes	Configuration Register Select
DACK[1:0]n	→		DMA Demand Mode Acknowledge
DMPAF	→		Direct Mast Programmable Almost Full
DP[3:0]	←→	yes	Data Parity
DREQ[1:0]n	←	yes	DMA Demand Mode Request
LA[31:2]	←→		Local Address Bus
LBEn[3:0]	←→		Local Bytes Enables
LD[31:0]	←→		Local Data Bus
LINTin	←	yes	Local Interrupt Input to PCI9056
LINTon	→	yes	Local Interrupt Output from PCI9056
LRESETn	→		Local Bus Reset

Signal	Direction PCI9056 ←→ FPGA	Pull up	Description
LSERRn	→		Local System Error Interrupt
LWRn	←→		Local Write/Read
READYn	←→	yes	Ready
WAITn	←→	yes	Wait

Table 5-4 : Local Bus Signals

5.5.2 Local Bus Arbitration

The Local Bus arbitration is performed by a local bus arbiter that is part of the JTAG-Controller CPLD. This arbiter prioritizes the PCI9056.

Signal	Pull up	Description
BACKOFF	-	Bus Backoff Request, PCI9056 BREQo
LGNTn	yes	Local Bus Grant
LREQn	yes	Local Bus Request
GTRI	-	Global Tristate

Table 5-5 : Local Bus Arbitration Signals

The FPGA can request the local bus by asserting LREQn. The local bus is granted to the FPGA when LGNTn is asserted. If the PCI9056 requests the local bus while it is granted to the FPGA, the arbiter will deassert LGNTn to signal the FPGA that it shall release the local bus. The arbiter waits until LREQn is deasserted by the FPGA and then grants the local bus to the PCI9056.

Additionally the Backoff Sequence of the PCI9056 can be used to prevent deadlocks on the local bus. The PCI9056's BREQo signal is forwarded as the BACKOFF-signal to the FPGA. Refer to the chapter "5.4.3.1 Backoff" of the PCI9056 Data Book.

5.6 DDR2 SDRAM

The TCP631 provides 2 banks of 128 Mbytes DDR2 RAM. Both banks are connected to the FPGA with a 16 bit data bus width.

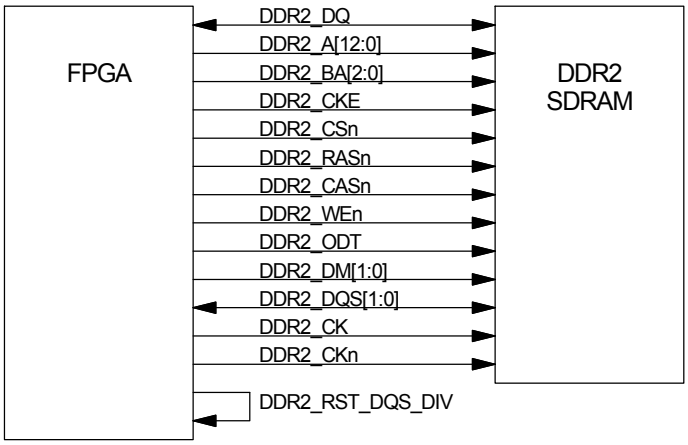

Figure 5-3 : DDR2 SDRAM Interface

For details regarding the DDR2 SDRAM interface, please refer to the DDR2 SDRAM Data Sheet and the Xilinx documentation. The TCP631 Engineering Documentation includes a DDR2 SDRAM example design.

5.7 JTAG

The TCP631 offers two JTAG-chains. JTAG-Chain 1 is user accessible and includes the user relevant devices. JTAG-Chain 2 is for factory use only.

5.7.1 JTAG-Chain 1

The FPGA, the platform flash and the programmable clock generator device are in-system programmable from the PCI bus. An on board JTAG-Controller provides access from the local bus to a JTAG chain including the FPGA, the platform flash and the programmable clock generator.

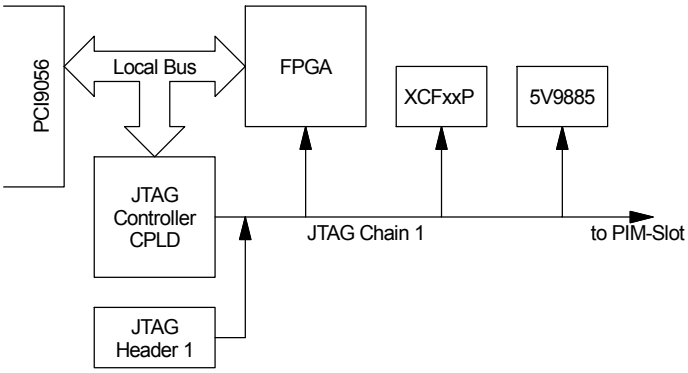

Figure 5-4 : In-System Programming

For FPGA readback or in-system diagnostics with ChipScope, alternatively the JTAG Header 1 can be used to access the JTAG-chain. The JTAG-chain can be extended to include the PIM Slot and the J2 connector, so JTAG capable PIM or transition modules can be used.

The on board JTAG-Controller is activated by asserting the PCI9056 USERo signal. While the JTAG-Controller is active, the FPGA is set in a “configuration reset” state, with pull-ups on the I/O-pins. When the JTAG-Controller is deactivated, the FPGA will automatically reconfigure. The FPGA’s DONE state can be observed on the PCI9056 USERi pin.

5.7.2 JTAG-Chain 1 Segmentation

To ease the use of JTAG-chain 1, it can be partitioned into segments. Each segment can be separately held inactive and thereby excluded (“bypassed”) from the chain. In this way it is possible to target a specific JTAG device which makes the use of the .svf generating software more convenient. It also allows masking the on board JTAG devices when a JTAG-device on a PIM slot or on J2 back I/O is targeted.

The first segment contains the FPGA and the configuration device. The second segment contains the clock generator. Selection of these segments is controlled by the on board JTAG-controller. The third segment contains the PIM Slot, and the last segment contains the J2 Back I/O. The latter two segments are only activated when a JTAG capable PIM or transition module is installed.

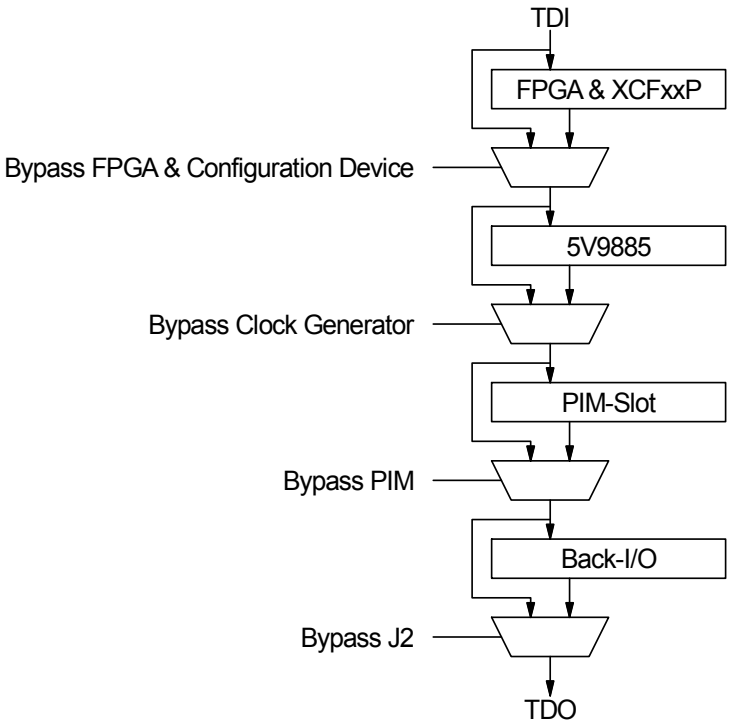

Figure 5-5 : JTAG-Chain 1 Segmentation

Devices in inactive segments are hold in the Test-Logic-Reset State. The FPGA/configuration device segment and the clock generator segment are active by default.

The PIM slot and J2 Back I/O are always bypassed, even with a JTAG-capable PIM or transition module, when the jumper J3 (PIM slot) and J4 (J2 Back I/O) are closed.

6 Configuration Hints

6.1 Configuration

The FPGA can be configured either from the platform flash or directly via the JTAG interface. When a JTAG configuration is desired, the “FPGA JTAG Configuration” bit in the Configuration PLD must be set. This bit changes the FPGA’s MODE pins from “Master parallel” mode to “JTAG Configuration” mode to prevent that the JTAG configuration is overwritten by the default configuration from the platform flash.

6.2 Configuration File Creation

6.2.1 FPGA & Configuration Device

6.2.1.1 Using Batches

The VHDL examples include two batch files. These batch files take the ISE .bit file and generate a .svf file using iMPACT:

- Run_Impact_PF: This batch file takes the projects .bit file and converts it to a .svf file which programs the configuration device.
- Run_Impact_FPGA: This batch file takes the projects .bit file and converts it to a .svf file for direct FPGA configuration.

Both batches do not include the clock generator device into the JTAG-chain. When using this .svf file, the clock generator must be excluded from the JTAG-chain and the TCP631 must not be connected to a JTAG-capable PIM or Transition module.

6.2.1.2 Using the iMPACT GUI

When using the iMPACT GUI to manually create the configuration files, some essential options in the Device Programming Properties must be set for Platform Flash configuration files:

PROM Specific Properties:

- Load FPGA (optional): When this option is set, once the PROM is configured the PROM toggles the FPGA’s program pin and configuration commences automatically.
- Parallel Mode: Since the XCFxxP PROM device is connected in a SelectMAP configuration, the parallel mode bit must be set, so that the PROM uses the DO-D7 pins for programming of the FPGA.

Advanced PROM Programming Properties

- During Configuration: PROM is Slave (clocked externally): Configuration is controlled by the FPGA

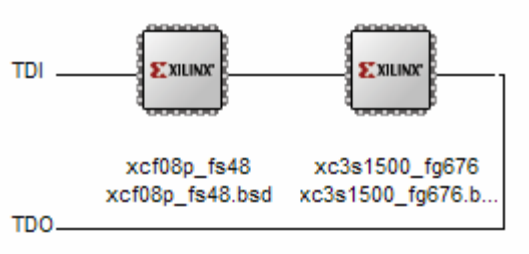

Figure 6-1 : This is how the JTAG-Chain should look like in iMPACT

Creating a SVF-file for direct FPGA programming:

- Create a new project
- “Prepare a Boundary-Scan File”
- Select the desired .bit-file
- “Add Xilinx Device” (At this point the BSDL-file of the platform flash device is needed. It can be found in %XILINX%\ISE\xcfp\data\xcf08p.bsd or on the Xilinx website.)
- “Program” the FPGA
- Close iMPACT.

Creating a SVF-file for the Platform Flash:

- Prepare a Platform Flash PROM File as described in UG332, Chapter 3: “Preparing a Platform Flash PROM File”
- Create a new project
- “Prepare a Boundary-Scan File”
- Select the prepared .mcs-file
- “Add Xilinx Device” (At this point the BSDL-file of the platform flash device is needed. It can be found in %XILINX%\ISE\spartan3\data\xc3s1500.bsd or on the Xilinx website.)
- Set the Programming Properties of the Platform Flash
- “Program” the Platform Flash
- Close iMPACT.

6.2.2 Clock Generator

The IDT5V9885C programmable clock generator can be programmed via the JTAG-Chain 1. IDT supplies the „IDT Programmable Clock“ programming software, which supports the export of the .svf file needed by the JTAG programming algorithms.

To use this .svf file, the FPGA and the configuration device must be bypassed and the TCP631 must not be connected to a JTAG-capable PIM or Transition module. The clock generator must be the only active segment of the JTAG-chain 1.

6.3 JTAG-Controller PLD

The on board JTAG-Controller PLD is activated by asserting the PCI9056 USERo signal. While the JTAG-Controller is active, the FPGA is set in a “configuration reset” state, with pull-ups on the I/O-pins. When the JTAG-Controller is deactivated, the FPGA will automatically reconfigure.

The JTAG-Controller PLD also gives access to a couple of board status signals, as power good signals from the power supplies.

The JTAG-Controller PLD expects 32-bit accesses without wait states. The JTAG-Controller PLD generates the READYn signal.

6.3.1 JTAG-Controller PLD Address Map

The JTAG-Controller PLD, when active, reacts to every local bus access. Thus it is accessible through Local Space 0 and Local Space 1.

Only 32 bit wide accesses are allowed.

Address	Register Description	Width	Access	Default (0x)
0x00	TAP Status / Configuration Register	32 bit	R/W	xxxx0800
0x04	Command Register	32 bit	R/W	xxxxF00F (xxxxD00F)
0x08	TDO Buffer	32 bit	R/W	00000000
0x0C	TCK Counter	32 bit	R/W	00000000
0x10	TDI Buffer	32 bit	R	00000000
0x14	Reserved	-	-	-
0x18	Reserved	-	-	-
0x1C	Board Status / Control	32 bit	R/W	xxxxF000

Table 6-1 : JTAG Controller PLD Address Map

6.3.2 TAP Status / Configuration Register

The TAP Status / Configuration Register shows the JTAG status and allows to configure the JTAG interface.

Bit	Symbol	Register Description	Access	Reset Value
31:16	-	Unused. Writes are ignored, reads are undefined.	R/W	-
15:12	TAP	TAP State Reflects the current TAP-Controller State: End State — Description 0000 — Test-Logic-Reset 0001 — Run-Test/Idle 0010 — Select-DR 0011 — Capture-DR 0100 — Shift-DR	R	0000

Bit	Symbol	Register Description	Access	Reset Value
		0101 Exit-DR 0110 Pause-DR 0111 Exit2-DR 1000 Update-DR 1001 Select-IR 1010 Capture-IR 1011 Shift-IR 1100 Exit-IR 1101 Pause-IR 1110 Exit2-IR 1111 Update-IR		
11	CNTR0	TCK Counter Status 0 = TCK Counter is loaded 1 = TCK Counter is zero	R	1
10:6	CLK DIV	Clock Divider Divide 48 MHz System Clock with this Value Divided Clock = 48 MHz / (2 x (1 + CLKDIV)) Must be ≥ 1	R/W	1
5	BPS4	Bypass J2 JTAG-chain segment 0 = Include J2 into JTAG-chain1. This segment is included only when a JTAG capable device is on J2. 1 = Bypass J2 (default '0' = Hardware control!) This setting is overridden when Jumper J3 is closed	R/W	0
4	BPS3	Bypass PIM JTAG-chain segment 0 = Include PIM into JTAG-chain1. This segment is included only when a JTAG capable device is on the PIM. 1 = Bypass PIM (default '0' = Hardware control!) This setting is overridden when Jumper J4 is closed	R/W	0
3	BPS2	Bypass Clock Generator JTAG-chain Segment 0 = Include Clock Generator into JTAG-chain1 1 = Bypass Clock Generator	R/W	0
2	BPS1	Bypass FPGA & Configuration Device JTAG-chain Segment 0 = Include FPGA & Configuration Device into JTAG-chain1 1 = Bypass FPGA & Configuration Device	R/W	0
1	TRIE	Tristate Outputs 0 = Tristate TCK, TMS, TDO, TRST	R/W	0

Bit	Symbol	Register Description	Access	Reset Value
		1 = Enable TCK, TMS, TDO, TRST This bit is automatically set to '0' when the CPLD is deselected.		
0	MODE	TCK Mode 0 = Gated TCK All TAP-Controller signals are under control of the TAP State machine. TCK is run when the TAP state transitions, otherwise it is gated off. 1 = Discrete Mode All TAP-Controller signals are under control of the Discrete bits in the Command Register	R/W	0

Table 6-2 : Status / Configuration Register

6.3.3 Command Register

In the Command Register the JTAG commands are issued.

Bit	Symbol	Register Description	Access	Reset Value
31:16	-	Unused. Writes are ignored, reads are undefined.	R/W	-
15	DTCK	Discrete TCK. Active when MODE = 1	R/W	1
14	DTMS	Discrete TMS. Active when MODE = 1	R/W	1
13	DTDI	Discrete TDI. Always reflects the TDI input	R	-
12	DTDO	Discrete TDO. Active when MODE = 1	R/W	1
10:8	-	Unused. Writes are ignored, reads are undefined.	R/W	-
7	ACTION	Action Request Indicates a valid OPCODE. Self-clearing bit, always reads as 0.	W	0
6	TRST	TRST# Pin Control 0 = TRST# is '0' 1 = TRST# is '1'	R/W	1

Bit	Symbol	Register Description	Access	Reset Value
5:4	ENDST	TAP End State The command given in OPCODE is finished in this TAP-controller state. This is influenced by the CONT bit in the TCK Counter Register. If CONT is set to '1', the TAP-controller stays in the SHIFT state until CONT is set to '0'. End State — Description 00 — Test-Logic-Reset 01 — Run-Test/Idle 10 — Pause-DR 11 — Pause-IR	R/W	0
3:0	OP CODE	OPCODE Operation to perform. OpCode — Description --00 — Instruction Register Scan --01 — Data Register Scan --10 — Run Test --11 — Test Logic Reset (sets TMS = 1, needs >5 TCK) Load the TCK Counter with at least 5 clock ticks for the Test Logic Reset Opcode. OPCODE[3:2] are don't care.	R/W	0xF

Table 6-3 : Command Register

6.3.4 TDO Buffer

Contains the Data that is put out on the TDO-line

Bit	Symbol	Register Description	Access	Reset Value
31:0	TDOB	TDO Buffer	R/W	0

Table 6-4 : TDO Buffer

6.3.5 TCK Counter

In the TCK Counter Register the number of TCK-clock ticks to put out is specified.

Bit	Symbol	Register Description	Access	Reset Value
31:9	-	Unused.	R/W	-

Bit	Symbol	Register Description	Access	Reset Value
		Writes are ignored, reads are undefined.		
8	CONT	Continue in SHIFT state 0 = Proceed to TAP End State when the TCK Counter is '0' 1 = Stay in SHIFT State when the TCK Counter is '0'	R/W	0
7:6	-	Unused. Writes are ignored, reads are undefined.	R/W	-
5:0	TCKC	TCK Counter Number of TCK ticks to output	R/W	0

Table 6-5 : TCK Counter

If the CONT-bit is used to split up a lengthy shift operation, the Command Register must only be set on the beginning of the shift operation. Afterwards it is only necessary to fill up the TDO Buffer and the TCK Counter to continue the shift. The shift operation is finished, when the CONT bit is set to '0'.

6.3.6 TDI Buffer

Contains the Data that is read in from the TDI-line

Bit	Symbol	Register Description	Access	Reset Value
31:0	TDIB	TDI Buffer	R/W	0

Table 6-6 : TDI Buffer

The read data is left-aligned. If a read was shorter than 32 bit, the TDI Buffer contains old data in the lower bits. These should be masked out when the TDI Buffer is evaluated.

6.3.7 Board Status / Command

In the Board Status / Command Register the status of the board is shown and commands on board level can be issued.

Bit	Symbol	Register Description	Access	Reset Value
31:16	-	Unused. Writes are ignored, reads are undefined.	R/W	-
15	2V5OK	2.5V Board Supply Power Good	R	-
14	1V8OK	1.8V Board Supply Power Good	R	-
13	1V2OK	1.2V Board Supply Power Good	R	-
12	0V9OK	0.9V Board Supply Power Good	R	-
11:6	-	Unused. Writes are ignored, reads are undefined.	R	-
5	INT STA	Interrupt Status & Acknowledge Write '1' to acknowledge the interrupt	R/W	0
4	INT EN	Enable Interrupts on TCK Counter = '0'.	R/W	0

Bit	Symbol	Register Description	Access	Reset Value
		Interrupts are acknowledged by set the TCK Counter to a non-zero value. Interrupt Status can be checked with the CNTR0 bit in the TAP Status / Command Register.		
3:2	REV SEL	Revision Select (not implemented)	R/W	0
1	ESEL	External Revision Select Enable (not implemented)	R/W	0
0	PROG	FPGA JTAG configuration This bit changes the FPGA's MODE pins from "Master parallel" mode to "JTAG" mode to prevent that the JTAG configuration is overwritten by the default configuration from the platform flash. 0: Configuration from platform flash 1: Configuration via JTAG-interface	R/W	0

Table 6-7 : Board Status / Command

7 Design Help

Custom FPGA designs can be developed using a commercial version like Xilinx ISE Foundation or the ISE WebPACK, the latter downloadable free of charge at www.xilinx.com/ise. Taking the VHDL examples provided with the Engineering Documentation would be a good basis. After implementing the logic, the resulting .svf file can be downloaded to the configuration flash by the driver.

The examples assume that the user possesses at least basic VHDL skills. TEWS can not provide design support beyond the provided examples.

7.1 FPGA Bank Usage

Bank	V_{CCO}	V_{REF}	Description
0	3.3V	-	PIM Slot I/O
1	3.3V	-	PIM Slot I/O
2	3.3V	-	J2 I/O
3	3.3V	-	J2 I/O
4	3.3V	-	PCI9056 Interface, Configuration Pins
5	3.3V	-	PCI9056 Interface, Configuration Pins
6	1.8V	0.9V	DDR2
7	1.8V	0.9V	DDR2

Table 7-1 : FPGA Bank Usage

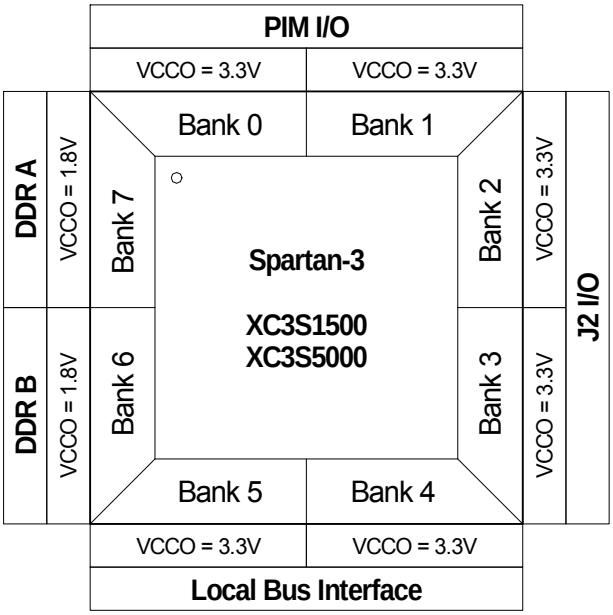

Figure 7-1 : FPGA Bank Usage

All I/O lines are directly connected to the FPGA-pins. All I/O lines provide external ESD-protection devices. The fixed V_{CCO} of 3.3V restricts the IOSTANDARD for PIM & J2 I/O to LVTTL or LVCMOS33. Refer to the Spartan-3 datasheet for Select I/O interface signal standards, slew rate control and current drive strength capabilities.

7.2 Example Designs

The example designs include an .ucf file with all necessary pin assignments and basic timing constraints. Also included is a VHDL top level entity template containing all TCP631 signals that are connected to the FPGA.

Refer to the Appendix of this User Manual for a description of the example designs.

7.2.1 Design Templates

A template for a direct slave and a direct master interface are provided. These templates contain all signals that are available in the FPGA. Each template is accompanied by an .ucf-file that contains the location constraints for all available signals, except for the DDR2 interfaces, and some basic timing constraints. The templates can be used as starting point for own designs.

When the DDR2 interfaces are used, each interface needs its own additional .ucf-file that contains the pin location, placement and timing constraints for the respective interface.

The templates and .ucf-files are included in the TCP631 Engineering Documentation.

7.3 Simulation & Verification

7.3.1 PCI9056

The example designs include a procedure based PCI9056 local bus simulation package which can be used to simulate Direct Slave Operation.

On request PLX offers a PCI9056 simulation model. The model requires a simulator that can handle SWIFT-based SmartModels, for example ModelSim SE. Note that the ModelSim XE simulator bundled with Xilinx ISE does not support the SWIFT Interface.

7.3.2 DDR2 RAM

7.3.2.1 Simulate DDR2 RAM Designs

The MIG generated DDR2 interfaces include a verilog simulation model supplied by Micron. Using this model with the VHDL based DDR2 interface requires a simulator with multi-language support, such as ModelSim SE or the ISE Simulator (ISIM). Alternatively the MT47H64M16 VHDL model from Free Model Foundry (www.freemodelfoundry.com) can be used to simulate the design in a VHDL-only simulator.

The TCP631 examples make use of the FMF MT47H64M16 VHDL model.

7.3.2.2 Verify Physical DDR2 Implementation

To successful implement the DDR2 memory interface, ISE needs specific process properties. Basically these are the default settings, with only following settings differing from the defaults:

Synthesis Options:

- Optimization Strategy (Cover Mode): Speed

Map Properties:

- Keep Hierarchy: Soft

If process properties are changed in ISE, the correct implementation of the DDR2 interface must be verified as described in UG086: “Xilinx Memory Interface Generator (MIG) User Guide” ("Debugging the Spartan-3 FPGA Design" -> "Verify Placement and Routing") or the Answer Records:

- #31107 (MIG v2.2 - Why is the environment variable "XIL_PAR_ALIGN_USER_RPMS" needed for Spartan-3 Generation DDR/DDR2 SDRAM designs, and can it be removed?)
- #25245 (MIG v2.0 - How do I determine whether the PAR template routes are properly used for Spartan-3 DDR/DDR2 SDRAM designs?).

7.4 Design Warnings

7.4.1 Designs Intended for FPGA JTAG Configuration

Designs that intended for direct FPGA configuration via JTAG without using the platform flash, must observe the “GTRI”-Signal.

When the FPGA is configured via JTAG, it becomes alive while the JTAG-Controller CPLD is still active. When GTRI is asserted, all FPGA outputs to the local bus must be tristated to avoid bus contentions with the active configuration CPLD.

8 Pin Assignment – I/O Connector

8.1 Header & Jumper

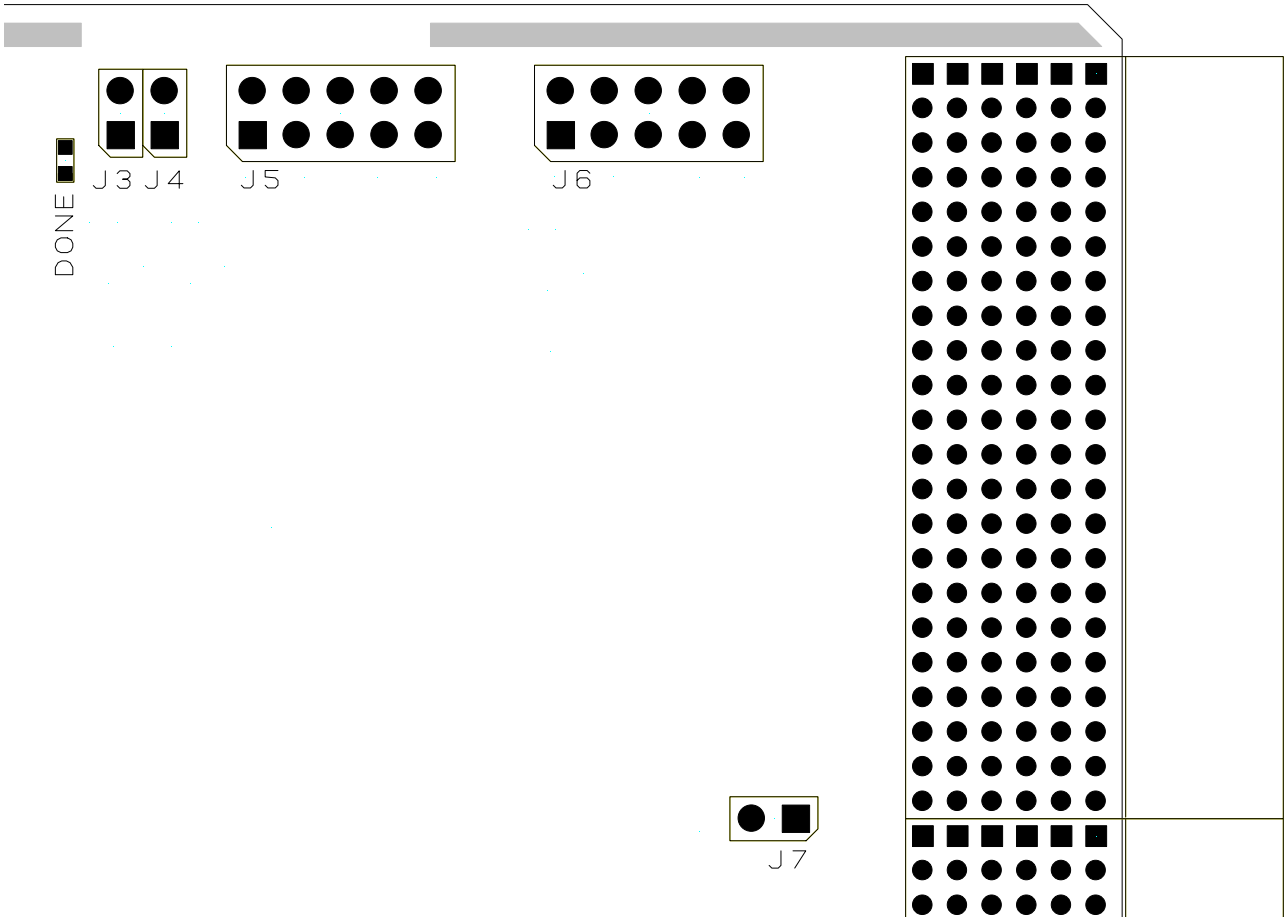

Figure 8-1 : Header & Jumper

8.1.1 Jumper

J3: Disable PIM JTAG

When this jumper is set, the PIM is excluded from the JTAG-chain 1, even when the PIM is JTAG-capable.

J4: Disable J2 JTAG

When this jumper is set, J2 back I/O is excluded from the JTAG-chain 1, even when the transition module is JTAG-capable.

J7: Inhibit FPGA Configuration

When this jumper is set, the FPGA's INIT_B pin is pulled low. This inhibits the FPGA configuration.

8.1.2 JTAG Header 1 (J5)

It lets the user directly connect a JTAG interface cable to the JTAG pins of the FPGA for readback and real-time debugging of the FPGA design (using Xilinx “ChipScope”).

Pin	Signal	Description
1	TCK	Test Clock
2	GND	Ground
3	TMS	Test Mode Select Input
4	GND	Ground
5	TDO	Test Data Output (TAP Controller: TDI)
6	GND	Ground
7	TDI	Test Data Input (TAP Controller: TDO)
8	GND	Ground
9	TRST#	Test Reset
10	-	not connected on the TCP631

Table 8-1 : Pin Assignment JTAG Header

8.1.3 JTAG Header 2 (J6)

The JTAG Header J6 is for factory use only.

8.2 PIM Slot Connectors

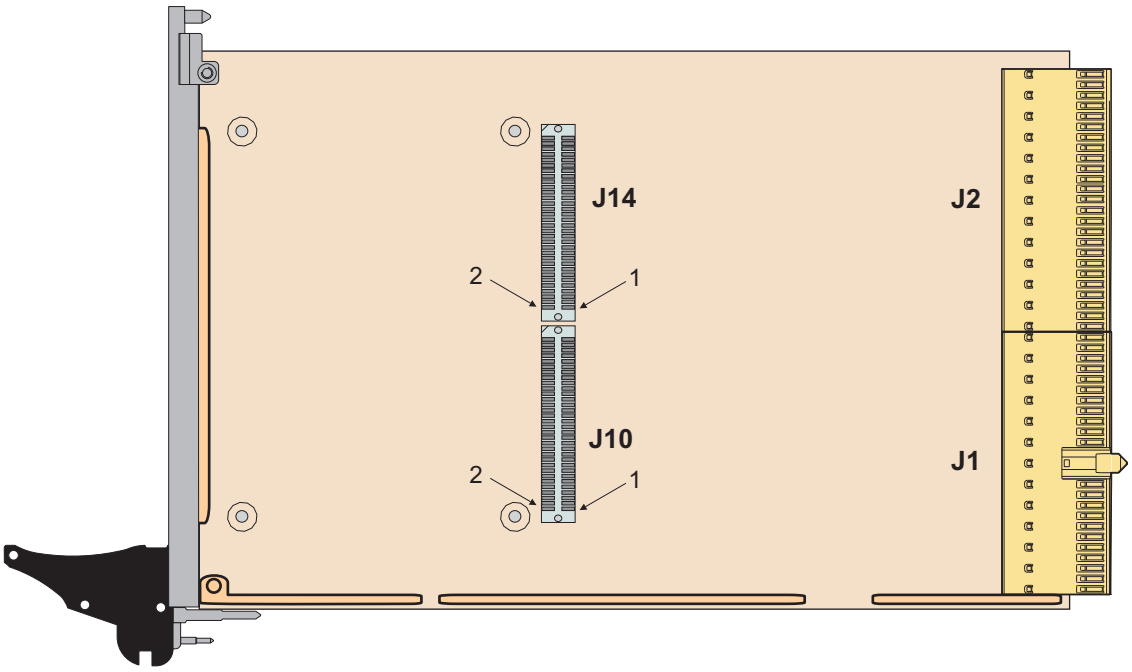

Figure 8-2 : Connector Positions

8.2.1 J10 Assignment

The PIM Slot offers a connection to the JTAG-Chain. The PIM Slot uses pins on the J10 connector for the JTAG signals (shaded in light yellow). This pin assignment is non-standard and special PIMs are required to use this signals on a PIM.

If a PIM shall be included in the JTAG-chain, it must tie “JTAG ENA” to GND.

Pin	Signal	Pin	Signal
1	TCK	2	+12V
3	TMS	4	TDI
5	+5V	6	TDO
7	TRST#	8	JTAG ENA#
9	-	10	+3.3V
11	-	12	-
13	GND	14	-
15	-	16	-
17	-	18	GND
19	-	20	-
21	+5V	22	-
23	-	24	-
25	-	26	+3.3V
27	-	28	-
29	GND	30	-
31	-	32	-
33	-	34	GND
35	-	36	-
37	+5V	38	-
39	-	40	-
41	-	42	+3.3V
43	-	44	-
45	GND	46	-
47	-	48	-
49	-	50	GND
51	-	52	-
53	+5V	54	-
55	-	56	-
57	-	58	+3.3V
59	-	60	-
61	-12V	62	-
63	-	64	-

Table 8-2 : Pin Assignment J10 Connector

8.2.2 J14 PIM Connector

Pin	Signal	FPGA Pin	Pin	Signal	FPGA Pin
1	IO_0	A10	2	IO_1	B3
3	IO_2	A11	4	IO_3	B4
5	IO_4	A12	6	IO_5	B5
7	IO_6	A14	8	IO_7	B6
9	IO_8	A15	10	IO_9	B7
11	IO_10	A16	12	IO_11	B8
13	IO_12	A17	14	IO_13	B9
15	IO_14	A19	16	IO_15	B10
17	IO_16	A20	18	IO_17	B11
19	IO_18	A21	20	IO_19	B12
21	IO_20	A22	22	IO_21	B13
23	IO_22	A23	24	IO_23	B14
25	IO_24	C21	26	IO_25	B15
27	IO_26	C22	28	IO_27	B16
29	IO_28	A3	30	IO_29	B17
31	IO_30	A4	32	IO_31	B18
33	IO_32	D9	34	IO_33	B19
35	IO_34	D10	36	IO_35	B20
37	IO_36	D11	38	IO_37	B21
39	IO_38	D13	40	IO_39	B22
41	IO_40	D14	42	IO_41	B23
43	IO_42	D16	44	IO_43	C4
45	IO_44	D17	46	IO_45	C5
47	IO_46	D18	48	IO_47	C6
49	IO_48	A5	50	IO_49	C8
51	IO_50	A6	52	IO_51	C9
53	IO_52	A7	54	IO_53	C10
55	IO_54	A8	56	IO_55	C13
57	IO_56	D5	58	IO_57	C15
59	IO_58	D6	60	IO_59	C17
61	IO_60	D7	62	IO_61	C18
63	IO_62	D8	64	IO_63	C19

Table 8-3 : Pin Assignment J14 PIM Connector

8.3 Back I/O J2 Connector

8.3.1 Back I/O Assignment TCP631-2x

The J2 Back I/O Connector offers a connection to the JTAG-Chain. The J2 Back I/O Connector uses the pins shaded in light yellow for the JTAG signals. This pin assignment is non-standard and special transition Modules are required to use this signals.

Pos.	F	E	D	C	B	A
22	GND	not used	not used	not used	not used	not used
21	GND	not used	not used	not used	not used	not used
20	GND	not used	not used	not used	not used	not used
19	GND	not used	not used	not used	not used	not used
18	GND	not used	not used	not used	not used	not used
17	GND	not used	not used	not used	not used	not used
16	GND	JTAG ENA	not used	not used	not used	not used
15	GND	TCK	TMS	TDI	TDO	TRST
14	GND	+5V	+5V	+3,3V	+3,3V	+3,3V
13	GND	IO_0 (G23)	IO_1 (H23)	IO_2 (H24)	IO_3 (C25)	IO_4 (C26)
12	GND	IO_5 (E23)	IO_6 (E24)	IO_7 (D25)	IO_8 (D26)	IO_9 (E25)
11	GND	IO_10 (E26)	IO_11 (G20)	IO_12 (G21)	IO_13 (F23)	IO_14 (F24)
10	GND	IO_15 (G22)	IO_16 (J25)	IO_17 (K21)	IO_18 (K22)	IO_19 (K23)
9	GND	IO_20 (K24)	IO_21 (K25)	IO_22 (K26)	IO_23 (L19)	IO_24 (L20)
8	GND	IO_25 (L21)	IO_26 (L22)	IO_27 (L25)	IO_28 (L26)	IO_29 (M19)
7	GND	IO_30 (M20)	IO_31 (M21)	IO_32 (AA22)	IO_33 (AA21)	IO_34 (AB24)
6	GND	IO_35 (AB23)	IO_36 (AC26)	IO_37 (AC25)	IO_38 (Y21)	IO_39 (Y20)
5	GND	IO_40 (AB26)	IO_41 (AB25)	IO_42 (AA24)	IO_43 (AA23)	IO_44 (Y23)
4	GND	IO_45 (Y22)	IO_46 (AA26)	IO_47 (AA25)	IO_48 (V25)	IO_49 (V24)
3	GND	IO_50 (U22)	IO_51 (U21)	IO_52 (U24)	IO_53 (U23)	IO_54 (U26)
2	GND	IO_55 (U25)	IO_56 (T20)	IO_57 (T19)	IO_58 (T22)	IO_59 (T21)
1	GND	IO_60 (T26)	IO_61 (T25)	IO_62 (R20)	IO_63 (R19)	VI/O

Table 8-4 : Pin Assignment J2 I/O Connector TCP631-20

9 Appendix

The Local Base Addresses given in these examples are the local bus addresses, i.e. the addresses seen by the FPGA. These address spaces are mapped to PCI address spaces whose base addresses are available in the PCIBAR2 (for Local Space 0) and PCIBAR3 (for Local Space 1) registers of the PCI9056. Refer to the chapter “PCI9056 Address Space Configuration”.

9.1 Example Design Full I/O

The full I/O example design is a simple 64 bit digital I/O with edge detection and configurable edge interrupts.

The local base address 0 gives access to the PIM and J2 I/O.

The local base address 1 is used for some registers controlling the front panel LEDs.

9.1.1 Address Map

Address	Register Description	Width	Access
Local Space 0 (Local Base Address 0x80000000, mapped from PCIBAR2)			
PIM I/O			
0x00	Lower Input Register	32 bit	R
0x04	Upper Input Register	32 bit	R
0x08	Lower Output Register	32 bit	R/W
0x0C	Upper Output Register	32 bit	R/W
0x10	Lower Output Enable Register	32 bit	R/W
0x14	Upper Output Enable Register	32 bit	R/W
0x18	Lower Positive Edge Interrupt Status Register	32 bit	R/W
0x1C	Upper Positive Edge Interrupt Status Register	32 bit	R/W
0x20	Lower Negative Edge Interrupt Status Register	32 bit	R/W
0x24	Upper Negative Edge Interrupt Status Register	32 bit	R/W
0x28	Lower Positive Edge Interrupt Enable Register	32 bit	R/W
0x2C	Upper Positive Edge Interrupt Enable Register	32 bit	R/W
0x30	Lower Negative Edge Interrupt Enable Register	32 bit	R/W
0x34	Upper Negative Edge Interrupt Enable Register	32 bit	R/W
J2 Back I/O			
0x40	Lower Input Register	32 bit	R
0x44	Upper Input Register	32 bit	R
0x48	Lower Output Register	32 bit	R/W
0x4C	Upper Output Register	32 bit	R/W
0x50	Lower Output Enable Register	32 bit	R/W
0x54	Upper Output Enable Register	32 bit	R/W
0x58	Lower Positive Edge Interrupt Status Register	32 bit	R/W
0x5C	Upper Positive Edge Interrupt Status Register	32 bit	R/W

Address	Register Description	Width	Access
0x60	Lower Negative Edge Interrupt Status Register	32 bit	R/W
0x64	Upper Negative Edge Interrupt Status Register	32 bit	R/W
0x68	Lower Positive Edge Interrupt Enable Register	32 bit	R/W
0x6C	Upper Positive Edge Interrupt Enable Register	32 bit	R/W
0x70	Lower Negative Edge Interrupt Enable Register	32 bit	R/W
0x74	Upper Negative Edge Interrupt Enable Register	32 bit	R/W
0x80	Version Register	32 bit	R/W
Local Space 1 (Local Base Address 0x00000000, mapped from PCIBAR3)			
PIM I/O			
0x00	LED Register	32 bit	R/W
0x04	LED Blink Frequency Register	32 bit	R/W

Table 9-1 : Example Design Full I/O Address Map

9.1.2 Register Abstract

9.1.2.1 Input Register

Bit	Register Description	Access	Reset Value
63:32	Reflects the state of the inputs. Can be used to read back the output signals.	R/W	0
31:0		R/W	0

Table 9-2 : Input Register

9.1.2.2 Output Register

Bit	Register Description	Access	Reset Value
63:32	Holds the values for the output transceivers that are put out, if the corresponding output enable signal is set in the Output Enable Register.	R/W	0
31:0		R/W	0

Table 9-3 : Output Register

9.1.2.3 Output Enable Register

Bit	Register Description	Access	Reset Value
63:32	Each Output Transceiver can be tristated, if the output enable bit is disabled. 0 = output disabled (tristate) 1 = output enabled	R/W	0
31:0		R/W	0

Table 9-4 : Output Enable Register

9.1.2.4 Positive Edge Interrupt Enable Register (PIER) & Negative Edge Interrupt Enable Register (NIER)

Bit	Register Description	Access	Reset Value
63:32	Each input line can generate an interrupt on a rising edge, if enabled here. 0 = interrupts on rising edge disabled 1 = interrupts on rising edge enabled	R/W	0
31:0		R/W	0

Table 9-5 : Positive Edge Interrupt Enable Register (PIER) & Negative Edge Interrupt Enable Register (NIER)

9.1.2.5 Positive Edge Interrupt Status Register (PISR) & Negative Edge Interrupt Status Register (NISR)

Bit	Register Description	Access	Reset Value
63:32	A WRITE of '1' to the PISR clears the corresponding interrupt bit. This register is updated, if the following is valid simultaneously: 1.) The line is an input (Output Enable has to be '0') 2.) a positive edge was detected 3.) interrupts are enabled for the corresponding input line	R/W	0
31:0		R/W	0

Table 9-6 : Positive Edge Interrupt Status Register (PISR) & Negative Edge Interrupt Status Register (NISR)

9.1.2.6 LED Register

Bit	Register Description	Access	Reset Value
31:8	These bits are unused. They read as 0 and are don't care for writes.	-	0
7:4	Enable LED blinking. If blinking is enabled, the enable bit determines if the LED blinks "positive" or "negative". If blinking is disabled, the active bit sets the state of the LED: 0 = blinking disabled 1 = blinking enabled	R/W	0xC
3:0	Enable LED 0 = LED off 1 = LED on Bit 0 – LED A (green) Bit 1 – LED A (red) Bit 2 – LED B (green) Bit 3 – LED B (red)	R/W	0x5

Table 9-7 : LED Register

9.1.2.7 LED Blink Frequency Register

Bit	Register Description	Access	Reset Value
31:8	These bits are unused. They read as 0 and are don't care for writes.	-	0
7:0	This register is the uppermost byte of the counter that does the clock division. The default counter value would be 0x03FFFFFF.	R/W	0x03

Table 9-8 : LED Blink Frequency Register

9.2 Example Simple DDR2

The Simple DDR2 example design shows how to access the DDR2 SRAM using the MIG generated DDR2 interface.

The local base address 0 is divided into 2 parts which give access to the DDR2 interfaces A and B.

The local base address 1 is occupied by a 2048 x 32 bit block RAM which can be used to ensure the correct function of local bus accesses.

The front panel LEDs are used as status indicators. If all LEDs are lit, both DDR2 interfaces are initialized, the DCM has locked und RST is deasserted.

9.2.1 Address Map

Address	Register Description	Width	Access
Local Space 0 (Local Base Address 0x80000000, mapped from PCIBAR2)			
0x000000: 0x7FFFF	DDR2 A	32 bit	R/W
0x800000: 0xFFFFF	DDR2 B	32 bit	R/W
Local Space 1 (Local Base Address 0x00000000, mapped from PCIBAR3)			
0x000: 0x7FF	Block RAM	32 bit	R/W

Table 9-9 : Example Design Simple DDR2 Address Map

9.3 Example Master

The Master example design showcases direct master configuration writes (using the CCSn signal), direct master writes and direct master reads. It automatically sets up the PCI9056 Direct Master-to-PCI registers and enables the Master Enable bit in the PCI9056's PCI Command register.

Local base address 0 is used as a trigger for the direct master operations:

- A WRITE to Local base address 0 copies 16 longwords from a ROM to PCI-Address 0x80000000.
- A READ to Local base address 0 copies 16 longwords from PCI-Address 0x80000000 to the block RAM in Local base address 1.

Local base address 1 is occupied by a 4096 x 32 bit block RAM which can be used to ensure the correct function of local bus accesses.

The green LED A is used as a direct slave access activity LED. The red LED A is used as direct master activity LED.

9.3.1 Address Map

Address	Register Description	Width	Access
Local Space 0 (Local Base Address 0x80000000, mapped from PCIBAR2)			
0x000000: 0xFFFFF	Trigger for the direct master operations	32 bit	R/W
Local Space 1 (Local Base Address 0x00000000, mapped from PCIBAR3)			
0x000: 0xFFF	Block RAM	32 bit	R/W

Table 9-10 : Example Design Simple DDR2 Address Map