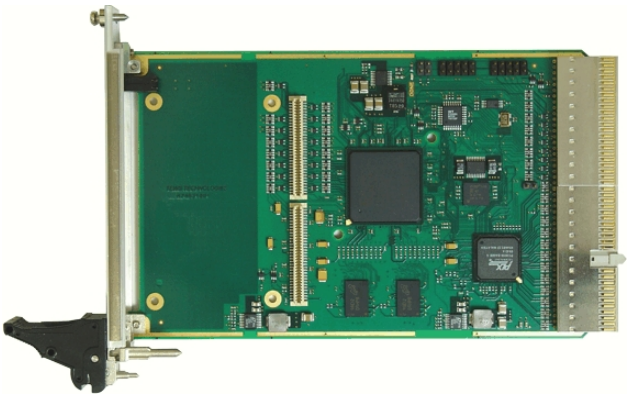
TCP631 Reconfigurable FPGA with direct Connect to PIM Module Slot

Application Information

The TCP631 is a standard 3U 32 bit CompactPCI module providing a user configurable FPGA with 1,500,000 or 5,000,000 system gates. All local signals from the PCI controller are routed to the FPGA.



The TCP631 offers 64 I/O lines to the front I/O and 64 I/O lines to the rear I/O. For flexible front I/O solutions the TCP631 provides a PIM Module slot, allowing active and passive signal conditioning. An option offers additionally 64 I/O lines via the J2 connector. All I/O lines are directly connected to the FPGA-pins, which maintains the flexibility of the Select I/O technology of the Spartan III FPGA. All I/O lines provide external ESD-protection devices. In addition the FPGA is connected to two banks of 128 Mbytes, 16 bit wide DDR2 SDRAM.

The FPGA is configured by a parallel flash. The flash device is in-system programmable via driver software over the PCI bus. An in-circuit debugging option is available via an optionally mountable JTAG header for readback and real-time debugging of the FPGA design (using Xilinx “ChipScope”).

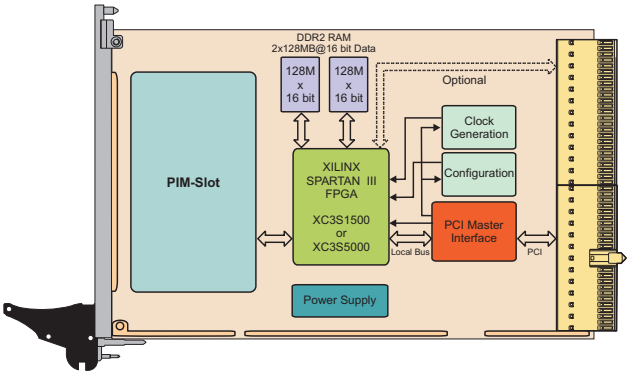
A programmable clock generator supplies up to four different clock frequencies between 5 kHz and 200 MHz which are available at the FPGA, in addition one clock source is used as the local clock signal for the PCI controller. The clock generator settings are stored in an EEPROM and can be changed by the driver software.

The configuration EEPROM of the PCI controller can also be modified by the driver software, to adapt address spaces etc.

User applications for the TCP631-x0 can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com. User applications for the TCP631-x1 require the full ISE Foundation software, which must be purchased from Xilinx.

Technical Information

- Form Factor: Standard 3U 32 bit CompactPCI module conforming to PICMG 2.0 R3.0
  - Board size: 160 mm x 100 mm
  - 32 bit PCI master interface by PLX PCI9056
  - PCI 2.2 compliant interface
  - 3.3V and 5V PCI Signaling Voltage
- Xilinx XC3S1500-4 Spartan-III or Xilinx XC3S5000-4 Spartan-III FPGA
- Flash device in-system programmable
- FPGA clock options:
  - Local clock oscillator
  - PLL programmable clock generator (5 KHz – 200 MHz), four clock outputs connected to FPGA
- 2x 128 Mbytes DDR2 RAM
- I/O access:
  64 I/O lines via a PIM Module slot,
  64 I/O lines on rear connector J2
- Operating temperature -40°C to +85°C



TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

Order Information

RoHS Compliant

TCP631-10R	Reconfigurable FPGA, 1,500k Gates
TCP631-11R	Reconfigurable FPGA, 5,000k Gates
TCP631-20R	Reconfigurable FPGA, 1,500k Gates, J2 rear I/O
TCP631-21R	Reconfigurable FPGA, 5,000k Gates, J2 rear I/O

None RoHS Compliant

TCP631-10	None RoHS compliant version of TCP631-10R
TCP631-11	None RoHS compliant version of TCP631-11R
TCP631-20	None RoHS compliant version of TCP631-20R
TCP631-21	None RoHS compliant version of TCP631-21R

Documentation

TCP631-DOC	User Manual
TCP631-ED	Engineering documentation (TCP631-DOC, Schematics, Assembly Drawing, Data Sheets, Example Code)

Software

TDRV014-SW-25	Integrity Software Support
TDRV014-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TDRV014-SW-65	Windows XP/XPE/2000 Software Support
TDRV014-SW-72	LynxOS Software Support
TDRV014-SW-82	LiNUX Software Support
TDRV014-SW-95	QNX 6 Software Support

For other operating systems please contact TEWS.

Related Products

TPIM003	PIM I/O Module with HD68 SCSI-3 type connector and special pin assignment
TCP001-FP-10	6U front panel extension for 3U cPCI boards

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com