
TCP872

CompactPCI Carrier for 2 CardBus / PC Card Cards

Version 1.0

User Manual

Issue 1.1

September 2006

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TCP872-10

CompactPCI Carrier with 2 Socket PC Card Interface, PC Cards accessible through front panel

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

| | |
|-----|------------|
| W | Write Only |
| R | Read Only |
| R/W | Read/Write |
| R/C | Read/Clear |
| R/S | Read/Set |

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| Issue | Description | Date |
|--------------|----------------------|----------------|
| 1.0 | First Issue | August 2004 |
| 1.1 | New address TEWS LLC | September 2006 |

Table of Contents

| | | |
|----------|--|-----------|
| 1 | PRODUCT DESCRIPTION | 6 |
| 2 | TECHNICAL SPECIFICATION | 7 |
| 3 | FUNCTIONAL DESCRIPTION | 8 |
| | 3.1 Address Mapping TCP872 – PC Card16 mode | 8 |
| | 3.1.1 Memory Mapping | 8 |
| | 3.1.2 I/O Mapping | 9 |
| | 3.2 Address Mapping TCP872 – CardBus mode | 10 |
| | 3.3 PCI Interrupts | 11 |
| 4 | PCI1520 PC CARD CONTROLLER | 12 |
| | 4.1 PCI Configuration Registers (Functions 0 and 1) | 12 |
| | 4.1.1 PCI Header of the TCP872 Version 1.0 | 12 |
| | 4.2 Configuration EEPROM | 13 |
| | 4.3 ISA Interrupts | 14 |
| | 4.4 Multifunction Pins | 15 |
| | 4.5 Initialization for CardBus mode | 16 |

Table of Figures

| | |
|---|----|
| FIGURE 1-1 : BLOCK DIAGRAM..... | 6 |
| FIGURE 2-1 : TECHNICAL SPECIFICATION..... | 7 |
| FIGURE 3-1 : PCI TO PC CARD MEMORY MAPPING | 8 |
| FIGURE 3-2 : PCI TO PC CARD I/O MAPPING | 9 |
| FIGURE 3-3 : CARDBUS WINDOW MECHANISM | 10 |
| FIGURE 3-4 : SOCKET REGISTERS IMPLEMENTED IN PCI1520 (FUNCTION 0 AND 1) | 10 |
| FIGURE 4-1 : PCI CONFIGURATION REGISTER | 12 |
| FIGURE 4-2 : CONFIGURATION EEPROM..... | 13 |
| FIGURE 4-3 : ISA INTERRUPTS | 14 |
| FIGURE 4-4 : POSITION OF X2 | 15 |
| FIGURE 4-5 : X2 SIGNAL ASSIGNMENT | 15 |

1 Product Description

The TCP872 is a standard 3U CompactPCI module with an interface for up to two 16 bit PC Card or 32 bit CardBus Cards using a dual socket PC Card controller and a power management unit. Up to two PC Card / CardBus Cards of Type I and II, or one card of Type III are supported. The register map of the PC Card controller is Intel 82365-DF compatible.

The TCP872 provides full ExCA register implementation for 16 bit PC Cards compatible with PCMCIA 2.1/JEIDA 4.2 standards. Both memory and I/O cards are supported. Up to five memory windows and up to two I/O windows are available for PC Card16 accesses. For 32 bit CardBus cards two memory windows and two I/O windows are supported by the controller. CardBus card status information can be accessed in five card bus socket registers which can be mapped in the host memory space.

The TCP872 can operate with 3.3V and 5.0V PCI I/O signaling voltage.

All CardBus / PC Card interrupt sources are mapped to PCI INTA.

The power management unit provides 3.3V or 5.0V PC Card power supply and 3.3V, 5.0V or 12V PC Card programming voltage. Due to the short circuit and thermal protection of the power management unit no external fuses are needed on the module.

The operating temperature range is -40°C to +85°C.

The TCP872 complies with the PICMG 2.0 Revision 3.0 CompactPCI specification.

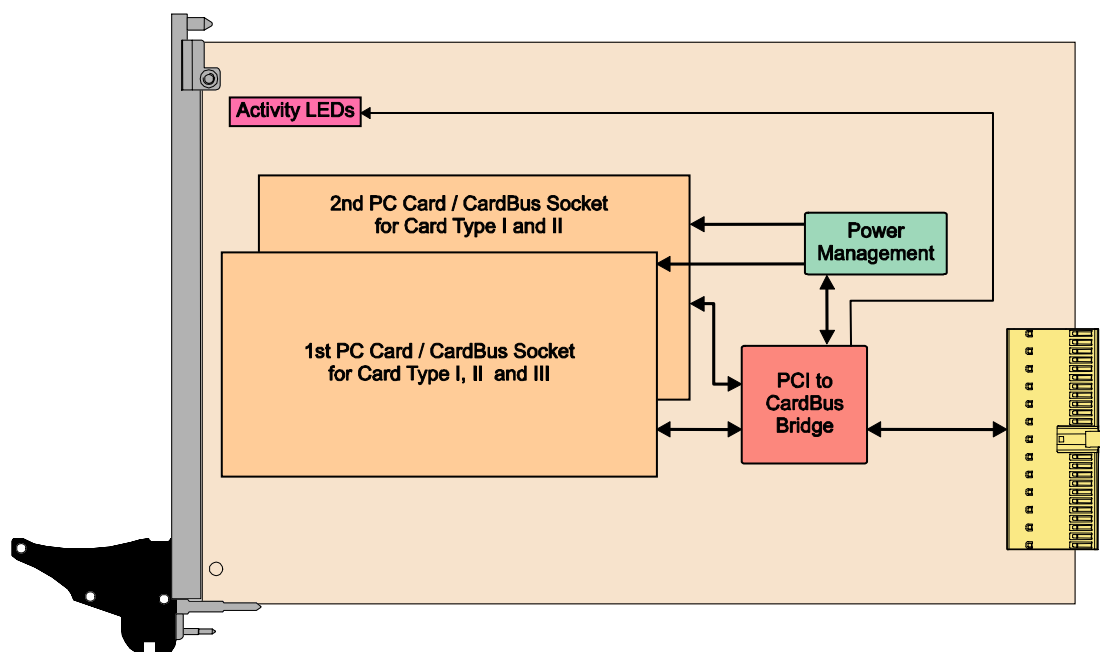


Figure 1-1 : Block Diagram

2 Technical Specification

| | | |
|--|--|----------------|
| Mechanical Interface | Compact PCI 3U, conforming to PICMG 2.0 R3.0 | |
| Electrical Interface | PCI Rev. 2.2 compliant interface, 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage | |
| On Board Devices | | |
| PCI Controller | Texas Instruments PCI1520 | |
| Module Specific Data | | |
| PC Card Interface | 16 bit PC Card electrical interface 32 bit CardBus electrical interface | |
| PC Card Sockets | 2 sockets for two cards of types I and II or one card of type III | |
| PC Card Operating Voltage | +3.3V or +5V | |
| PC Card Programming Voltage | +3.3V/+5V or +12V | |
| PC Card Supply Current | 1A maximum per socket | |
| PC Card Programming Current | 100mA maximum per socket | |
| Physical Data | | |
| Power Requirements | 70mA typical @ +3.3V DC 7mA typical @ +5V DC <2mA typical @ V(I/O) | |
| Power Requirements with PC Card | Voltage and current depends on the used PC Card | |
| Temperature Range | Operating | -40°C to +85°C |
| | Storage | -40°C to +85°C |
| MTBF | 503000 h | |
| Humidity | 5 – 95 % non-condensing | |
| Weight | 147 g, no PC Card inserted | |

Figure 2-1 : Technical Specification

3 Functional Description

The TCP872 uses a PCI1520 controller from Texas Instruments to support 16 bit PC Card16 and 32 bit CardBus Cards. The PCI1520 is a PCI-to-CardBus controller that supports two independent card sockets compliant with the PC Card Standard 7.1. For 16 bit PC Card control the PCI1520 is fully register compatible with the Intel 82365L-DF PC Card interface controller through the ExCA register set. The ExCA registers can be accessed indirectly via PCI I/O access space or directly via PCI memory address space.

3.1 Address Mapping TCP872 – PC Card16 mode

The PCI1520 provides a window mechanism to link the PCI space to PC Card16 address space. Memory and I/O windows are programmable by the host software in the ExCA registers of the PCI1520.

3.1.1 Memory Mapping

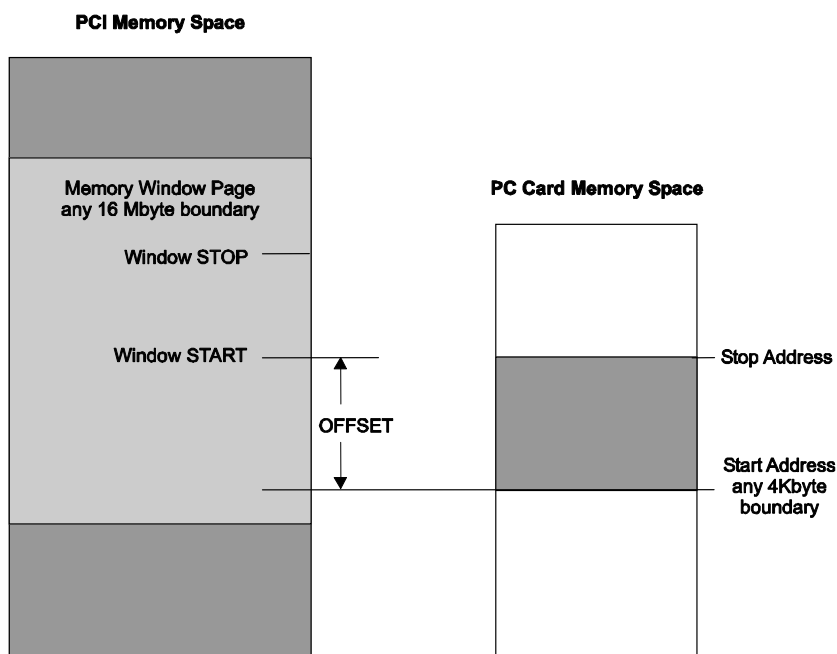


Figure 3-1 : PCI to PC Card memory mapping

To open a memory window, software must provide the PCI1520 with memory start address, memory stop address, PC Card memory offset and memory window page address.

PC Card memory is accessed only if the address window is enabled and if the memory address is located between start and stop address.

The Memory Window Page Register is only accessible via the PCI memory address space.

3.1.2 I/O Mapping

The 16 bit I/O card address space is accessed via 16 bit I/O addresses. The PC Card16 I/O space is mapped to the lower 64 kByte PCI I/O address space.

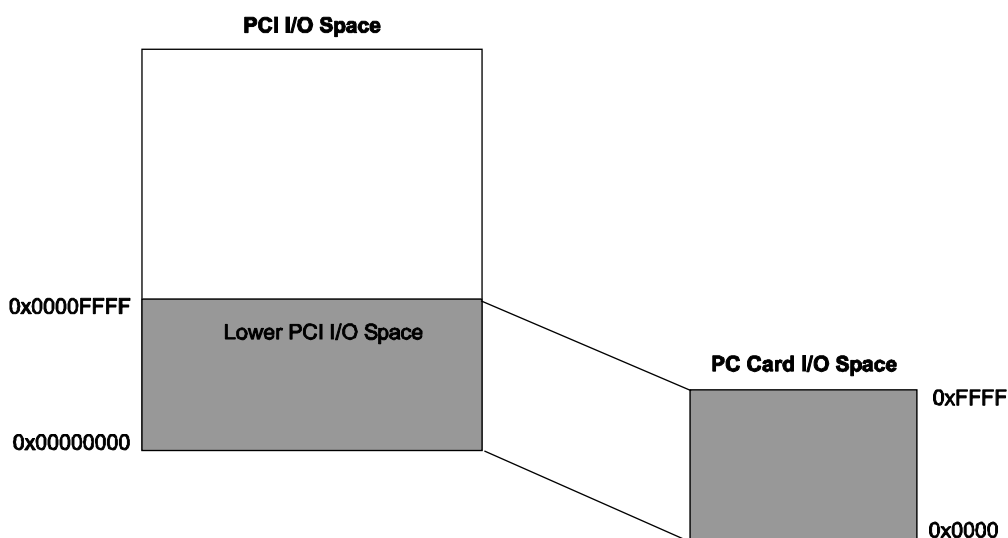


Figure 3-2 : PCI to PC Card I/O mapping

To open I/O window, software must provide the PCI1520 with I/O start address, I/O stop address, and I/O offset.

PC Card16 I/O is accessed only if the address window is enabled and if the I/O address is located between start and stop address.

For detailed information about window mapping procedure and status / control registers please refer to the PCI1520 data sheet which is part of the TCP872-ED Engineering Documentation.

3.2 Address Mapping TCP872 – CardBus mode

The PCI1520 provides a window mechanism to link the PCI space to 32 bit CardBus cards address spaces. Memory and I/O windows are programmable by the host software in the memory or I/O Base Registers in the PCI1520 configuration space. The PCI1520 offers two memory and two I/O windows per socket. The size of each window will be determined by host software via memory and I/O limit registers. The Base Address Registers will be initialized with the start addresses and the limit registers will be initialized with the upper address of the memory or I/O windows.

The CardBus card address space can be accessed via the CardBus base address registers, which are located in the PCI configuration space of the PCI1520.

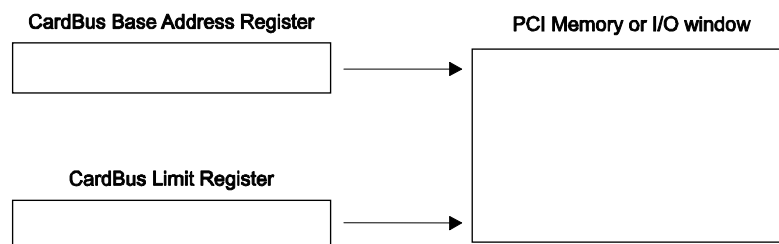


Figure 3-3 : CardBus window mechanism

The PCI1520 provides CardBus card status information via the CardBus Socket Register at configuration space offset 0x10. This address, which must be initialized by the device driver software, points to five 32 bit registers, which can be located anywhere in the PCI memory space at a 1 Kbytes boundary at offset 0x00. Each socket has a separate base address register to access the CardBus socket registers. The following socket registers are implemented in the PCI1520:

| Register Name | Offset |
|-------------------------|--------|
| Socket Event | 0x00 |
| Socket Mask | 0x04 |
| Socket Present State | 0x08 |
| Socket Force Event | 0x0C |
| Socket Control | 0x10 |
| Reserved | 0x14 |
| Reserved | 0x18 |
| Reserved | 0x1C |
| Socket Power Management | 0x20 |

Figure 3-4 : Socket Registers implemented in PCI1520 (Function 0 and 1)

These registers may notify the device driver software that a card has been inserted, removed, and what supply voltage is needed to power the CardBus card properly etc.

Further information regarding the status of the CardBus interface can be obtained from the secondary status register at offset 0x16 in the PCI configuration space of the PCI1520. This register is very similar to the PCI Bus Status Register and provides information about parity errors, aborted transactions, CardBus system errors etc.

For detailed register description, please refer to PCI1520 data sheet which is part of the TCP872-ED Engineering Documentation.

3.3 PCI Interrupts

The multifunction pin 0 of the PC Card socket controller is used as the PCI interrupt INTA#. The PCI1520 provides a card status change interrupt which can notify the system of change in the PC Card battery voltage levels, PC Card insertion / removal detection, Ready/Busy# condition and functional status change for both sockets. These various interrupt sources of both PC Cards are individually programmable to INTA# via ExCA "Card Status Change Interrupt Configuration Register" at ExCA register offset 0x05.

4 PCI1520 PC Card Controller

4.1 PCI Configuration Registers (Functions 0 and 1)

4.1.1 PCI Header of the TCP872 Version 1.0

| PCI CFG Register Address | | | | | | | | PCI write able | Read after Reset (Hex-Value) | |
|--------------------------|--|----|--------------------------|----|---------------------------------|-------------|--------------------|----------------|------------------------------|----------|
| | 31 | 24 | 23 | 16 | 15 | 8 | 7 | | | 0 |
| 0x00 | Device-ID | | | | Vendor-ID | | | | N | AC55104C |
| 0x04 | Status | | | | Command | | | | Y | 02100000 |
| 0x08 | Class Code | | | | | Revision ID | | | N | 06070001 |
| 0x0C | BIST | | Header Type | | PCI Latency Timer | | Cache line Size | | Y[7:0] | 00820000 |
| 0x10 | CardBus Socket/ExCA Base Address | | | | | | | Y | 00000000 | |
| 0x14 | Secondary Status | | | | Reserved | | Capability Pointer | | N | 020000A0 |
| 0x18 | CardBus Latency Timer | | Subordinate Bus Number | | CardBus Bus Number | | PCI Bus Number | | Y | 00000000 |
| 0x1C | CardBus Memory Base Register 0 | | | | | | | Y | 00000000 | |
| 0x20 | CardBus Memory Limit Register 0 | | | | | | | Y | 00000000 | |
| 0x24 | CardBus Memory Base Register 1 | | | | | | | Y | 00000000 | |
| 0x28 | CardBus Memory Limit Register 1 | | | | | | | Y | 00000000 | |
| 0x2C | CardBus I/O Base Register 0 | | | | | | | Y | 00000000 | |
| 0x30 | CardBus I/O Limit Register 0 | | | | | | | Y | 00000000 | |
| 0x34 | CardBus I/O Base Register 1 | | | | | | | Y | 00000000 | |
| 0x38 | CardBus I/O Limit Register 1 | | | | | | | Y | 00000000 | |
| 0x3C | Bridge Control Register | | | | Interrupt Pin | | Interrupt Line | | Y | 034001FF |
| 0x40 | Subsystem ID | | | | Subsystem Vendor ID | | | | Y | 23681498 |
| 0x44 | PC Card16 I/F legacy mode base address | | | | | | | Y | 00000001 | |
| 0x48-0x7C | Reserved | | | | | | | N | 00000000 | |
| 0x80 | System Control | | | | | | | Y | 2844D061 | |
| 0x84 | Reserved | | | | | | | N | 00000000 | |
| 0x8C | Multifunction Routing | | | | | | | Y | 00C01D02 | |
| 0x90 | Diagnostic | | Device Control | | Card Control | | Retry Status | | Y | 616400C0 |
| 0x94 | Reserved | | | | | | | Y | 00000000 | |
| 0x98 | Reserved | | | | | | | Y | 00000000 | |
| 0x9C | Reserved | | | | | | | N | 00000000 | |
| 0xA0 | Power Management Capabilities | | | | Next Item Pointer | | Capability ID | | N | 7E120001 |
| 0xA4 | PM data | | PMCSR bridge support | | Power Management status/control | | | | Y | 00C00000 |
| 0xA8 | General Purpose Event Enable | | | | General Purpose Event Status | | | | Y | 00000000 |
| 0xAC | General Purpose Output | | | | General Purpose Input | | | | Y | 00000000 |
| 0xB0 | Serial Bus Control /Status | | Serial Bus Slave Address | | Serial Bus Index | | Serial Bus Data | | Y | 00000000 |
| 0xB4-0xFC | Reserved | | | | | | | N | 00000000 | |

Figure 4-1 : PCI Configuration Register

4.2 Configuration EEPROM

The TCP872 is equipped with an on board I²C EEPROM. After power-on or PCI reset, the following PCI Configuration Register of the PCI1520 PC Card controller will be initialized with hardware depended configuration data:

| Register Name | Register Offset | EEPROM Offset | Value |
|----------------------------------|-------------------------------|---------------|------------|
| Load EEPROM Data Flag | - | 0x00 | 0x01 |
| Command Register | PCI 0x04 | 0x01 | 0x00 |
| Subsystem Vendor ID Register | PCI 0x40 | 0x02 | 0x1498 |
| Subsystem ID Register | PCI 0x42 | 0x04 | 0x2368 |
| PC Card16-I/F LBAR | PCI 0x44 | 0x06 | 0x00000001 |
| System Control Register | PCI 0x80 | 0x0A | 0x28D061 |
| Multifunction Routing Register | PCI 0x8C | 0x0D | 0x00C01D02 |
| Retry Status Register | PCI 0x90 | 0x11 | 0xC0 |
| Card Control Register | PCI 0x91 | 0x12 | 0x00 |
| Device Control Register | PCI 0x92 | 0x13 | 0x64 |
| Diagnostic Register | PCI 0x93 | 0x14 | 0x61 |
| Power Management Capability | PCI 0xA2 | 0x15 | 0x7E |
| ExCA Identification and Revision | ExCA 0x00 | 0x16 | 0x84 |
| Socket force Event (Function 0) | CB Socket + 0x0C (function 0) | 0x17 | 0x00 |
| Socket force Event (Function 1) | CB Socket + 0x0C (function 1) | 0x18 | 0x00 |

| Address | Offset | | | | | | | | | | | | | | | |
|---------|--------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| | 0x0 | 0x1 | 0x2 | 0x3 | 0x4 | 0x5 | 0x6 | 0x7 | 0x8 | 0x9 | 0xA | 0xB | 0xC | 0xD | 0xE | 0xF |
| 0x00 | 0x01 | 0x00 | 0x98 | 0x14 | 0x68 | 0x23 | 0x01 | 0x00 | 0x00 | 0x00 | 0x61 | 0xD0 | 0x28 | 0x02 | 0x1D | 0xC0 |
| 0x10 | 0x00 | 0xC0 | 0x00 | 0x64 | 0x61 | 0x7E | 0x84 | 0x00 | 0x00 | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |

Figure 4-2 : Configuration EEPROM

4.3 ISA Interrupts

The TCP872 provides a possibility to gain access to parallel or serialized ISA IRQ signals on board.

With the default EEPROM download configuration the PCI1520 is initialized to generate serial ISA IRQs on MFUNC3. For other IRQ configurations, the PCI1520 PC Card controller must be initialized through the controller's device driver. Interrupt signaling can be provided through the PCI1520 multifunction pins MFUNC3 and MFUNC6. MFUNC3 can be configured to function as serial or parallel ISA IRQ 2 to 15. MFUNC6 can be configured to function as parallel ISA IRQ 2 to 15. To enable the parallel ISA IRQs on these pins the following settings must be done by software:

| Register | Offset | Required Value | ISA Routing |
|------------------------|--------|-----------------------|---|
| Multifunction routing | 0x8C | Bits 27-24: 0x2 - 0xF | MFUNC6 is IRQ 2 -15 |
| Multifunction routing | 0x8C | Bits 15-12: 0x2 - 0xF | MFUNC3 is IRQ 2 -15 |
| Device control | 0x92 | Bits 2-1: 0x01 | Parallel ISA and PCI interrupts enabled |
| ExCA interrupt control | 0x03 | Bits 3-0: 0x3-0xF | IRQ 3-15 enabled |

Figure 4-3 : ISA Interrupts

For further information please refer to the PCI1520 data sheet which is part of the TCP872-ED Engineering Documentation.

The ISA IRQ signal of MFUNC3 can be accessed by routing the signal via a 0 ohm resistor to the CompactPCI connector J1 Pin E4. The IRQ signal of MFUNC6 can be accessed by routing the signal via a 0 ohm resistor to the CompactPCI connector J1 Pin D4.

4.4 Multifunction Pins

The PCI1520 provides several multifunction pins. On the TCP872 these multifunction pins are used for EPROM access, PCI INTA interrupt signaling and other purposes. The multifunction pins can be programmed to other functions by software. To provide access to the multifunction signals of the PCI1520, the TCP872 provides a 10 pin flat cable header:

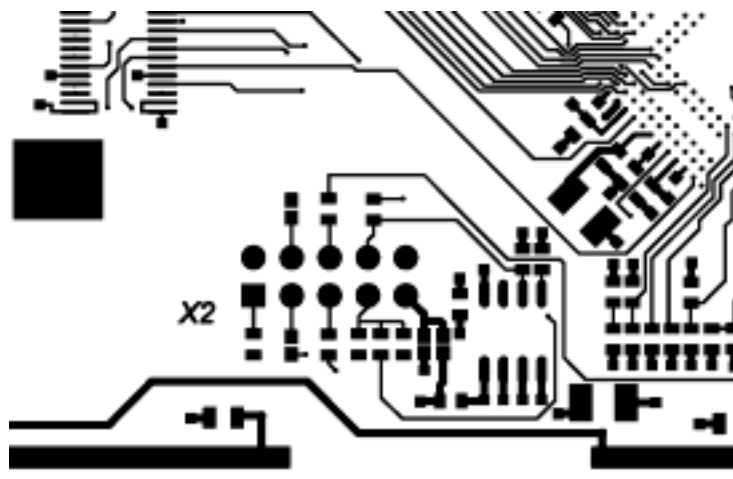


Figure 4-4 : Position of X2

| X2 | Signal | Default Function |
|--------------------|------------------|-----------------------|
| Pin 1 (square pad) | MFUNC5 | activity LED Socket 0 |
| Pin 2 | SPKROUT | - |
| Pin 3 | MFUNC6 / CLKRUN# | - |
| Pin 4 | MFUNC3 / IRQSER | - |
| Pin 5 | RI_OUT# / PME# | - |
| Pin 6 | MFUNC1 | SDA |
| Pin 7 | MFUNC2 | activity LED Socket 1 |
| Pin 8 | MFUNC4 | SCL |
| Pin 9 | 3,3V or 5V | - |
| Pin 10 | GND | GND |

Figure 4-5 : X2 Signal Assignment

4.5 Initialization for CardBus mode

The TCP872 is initialized for PC Card16 mode per default. If 32 bit CardBus operation is wanted, a software device driver should perform the following initialization steps:

- The CardBus Latency Timer Register at offset 0x1B in the PCI Configuration space should be set to a value of 0x20.
- A Memory and/or the I/O Base Address Register must be written with a valid 32 bit window start address.
- A Memory and/or I/O Limit Register must be written with a valid 32 bit upper window address.