The Embedded I/O Company

TEWS TECHNOLOGIES

TIP550

Optically Isolated 8/4 Channel 12-bit D/A

Version 1.2

User Manual

Issue 1.2.0

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TIP550-10

Optically Isolated 8 channel 12-bit D/A

TIP550-11

Optically Isolated 4 channel 12-bit D/A

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	February 1996
1.1	Technical Specification	April 1996
1.2	Register Description	December 1996
1.3	Status Register and General Revision	October 2002
1.4	DAC Control Register Description	October 2003
1.5	New Address: TEWS LLC	September 2006
1.2.0	New Hardware Revision of TIP550 New notation of User Manual Issue Corrected Jumper Configuration Figure	October 2009

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1 Product Description

The TIP550 is an IndustryPack® compatible module and provides 8 (TIP550-10) or 4 (TIP550-11) channels of isolated 12-bit D/A channels. The settling time to 0.01% is 13µs typical. The programmable output voltage range is +/-10V or 0-10V selectable by jumpers for each group of four D/A channels. The isolated DACs and the output buffers are powered by on board DC/DC converters.

Each TIP550 is factory calibrated. The calibration information for each D/A channel is stored in the Identification-PROM unique to each IP module.

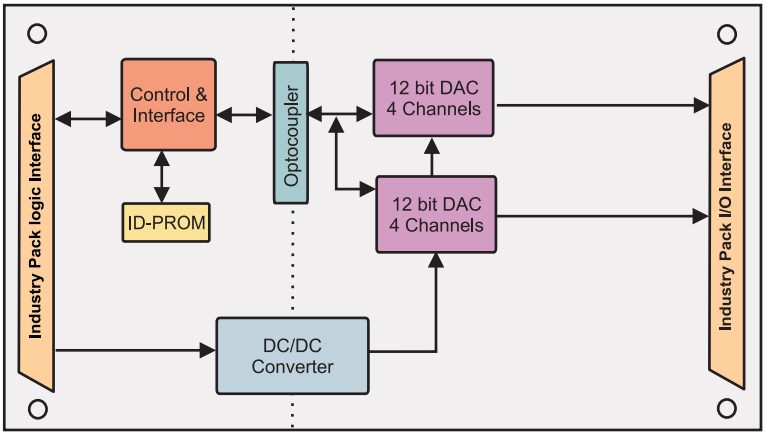

Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID PROM Data	Format I	
I/O Space	Used with 0 wait states	
Interrupts	INTREQ0 used, interrupt acknowledgement with 0 wait states	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
On Board Devices		
D/A Converter	DAC8420 (Analog Devices)	
Digital-to-Analog Conversion		
Resolution	12 Bit	
Output Voltage Range	0V…10V or ±10V, selectable for a group of four channels	
Output Settling Time	13µs typical to 0.01% from +10V to -10V	
Output Load per Channel	Max. ±4mA for each Channel	
I/O Interface		
Number of Channels	TIP550-10: 8 channels (in two groups of four channels) TIP550-11: 4 channels (in one group of four channels)	
Isolation	All D/A channels are optically isolated from the IP interface	
Interface Connector	50-conductor flat cable	
Power Requirements	TIP550-10: 350mA typical @ +5V DC ±12V DC: not used TIP550-11: 270mA typical @ +5V DC ±12V DC: not used	
Physical Data		
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +125°C
MTBF	TIP550-10: 639000 h TIP550-11: 724000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TIP550-10: 32 g TIP550-11: 31 g	

Table 2-1 : Technical Specification

3 ID PROM Contents

Address	Function	Contents
0x01	ASCII 'I'	**0x49**
0x03	ASCII 'P'	**0x50**
0x05	ASCII 'A'	**0x41**
0x07	ASCII 'C'	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x19**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x1D**
0x17	CRC	**Board dependent**
0x19	Version	**TIP550-10: 0A** **TIP550-11: 0B**
0x1B	Offset – DAC Channel 1	**Board dependent**
0x1D	Offset – DAC Channel 2	**Board dependent**
0x1F	Offset – DAC Channel 3	**Board dependent**
0x21	Offset – DAC Channel 4	**Board dependent**
0x23	Offset – DAC Channel 5	**Board dependent (TIP550-11x: 0x00)**
0x25	Offset – DAC Channel 6	**Board dependent (TIP550-11x: 0x00)**
0x27	Offset – DAC Channel 7	**Board dependent (TIP550-11x: 0x00)**
0x29	Offset – DAC Channel 8	**Board dependent (TIP550-11x: 0x00)**
0x2B	Gain – DAC Channel 1	**Board dependent**
0x2D	Gain – DAC Channel 2	**Board dependent**
0x2F	Gain – DAC Channel 3	**Board dependent**
0x31	Gain – DAC Channel 4	**Board dependent**
0x33	Gain – DAC Channel 5	**Board dependent (TIP550-11x: 0x00)**
0x35	Gain – DAC Channel 6	**Board dependent (TIP550-11x: 0x00)**
0x37	Gain – DAC Channel 7	**Board dependent (TIP550-11x: 0x00)**
0x39	Gain – DAC Channel 8	**Board dependent (TIP550-11x: 0x00)**
…	…	**…**
0x3F		**0x00**

Table 3-1 : ID PROM Contents

The VRGx bits in the DAC Control Register select the correct set of ID PROM calibration data values. Therefore, these bits have to be configured prior to reading any calibration data values from the ID PROM and also before starting any data conversion.

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP550 is accessible in the I/O space of the IP Module.

Address	Symbol	Description	Size (Bit)	Access
0x01	CHANSEL	DAC Channel Select Register	8	R/W
0x03	STATREG	DAC Status Register	8	R
0x04	DATAREG	DAC Data Register	16	R/W
0x07	INTVEC	Interrupt Vector Register	8	R/W
0x0B	CONTREG	DAC Control Register	8	R/W

Table 4-1 : IO Space Register Set TIP550

4.2 DAC Channel Select Register (Address: 0x01)

The DAC Channel Select Register (CHANSEL) is used to select an output channel. The write access that selects the channel also starts the serial data transfer to the DAC with the value stored in the DAC Data Register (DATAREG). Therefore, be sure that the desired value is stored inside the DATAREG prior to starting the conversion.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7:3</td><td>-</td><td>Not used, always read as ‘0’.</td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>CS2</td><td rowspan="3">Output Channel Selection:
<table>
<tr><th>CS2</th><th>CS1</th><th>CS0</th><th>Channel</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3</td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>5</td><td>TIP550-10 only</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6</td><td>TIP550-10 only</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>7</td><td>TIP550-10 only</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>8</td><td>TIP550-10 only</td></tr>
</table></td><td rowspan="3">R/W</td><td rowspan="3">000</td></tr>
<tr><td>1</td><td>CS1</td></tr>
<tr><td>0</td><td>CS0</td></tr>
</table>

Table 4-2 : DAC Channel Select Register (CHANSEL)

Always check that the DAC_BUSY flag is clear in the DAC Status Register (STATREG) before writing to the DAC Channel Select Register.

The TIP550-11x provides only four output channels. Therefore, Bit 2 of the DAC Channel Select Register must be ‘0’ for the TIP550-11x.

4.3 DAC Status Register (Address: 0x03)

The DAC Status Register (STATREG) provides status flags for the DAC communication.

Bit	Symbol	Description	Access	Reset Value
7:2	-	Not used, always read as '0'.	R	0
1	DATA_BUSY	Data Busy Flag: Indicates that a data value written into the DAC Data Register has not yet been transferred to the DAC. The data transfer is started by writing to the DAC Channel Select Register. This Bit is automatically set to '1' when a data value is written to the DATAREG. This Bit is automatically set to '0' when a transfer to the DACs is started by writing to the CHANSEL Register.	R	0
0	DAC_BUSY	DAC Busy Flag: Indicates that a serial data transfer to one of the DACs is in progress. This Bit is automatically set to '1' when a transfer to the DACs is started by writing to the CHANSEL Register. This Bit is automatically set to '0' when the current transfer is finished. Always check this flag before writing to the CHANSEL Register. 1 = Serial data transfer in progress 0 = No serial data transfer in progress	R	0

Table 4-3 : DAC Status Register (CHANSEL)

4.4 DAC Data Register (Address: 0x04)

The DAC Data Register (DATAREG) is a 12-bit wide read/write register. It contains the desired DAC conversion value.

Bit	Symbol	Description	Access	Reset Value
15:12	-	Not used, always read as '0'.	R/W	0
11:0	DAC_DATA	12-bit DAC value to be converted.	R/W	0x0000

Table 4-4 : DAC Data Register (DATAREG)

Always check that the DATA_BUSY flag in the DAC Status Register is clear before writing to the DAC Data Register.

For DAC data coding see chapter "DAC Data Coding".

4.5 Interrupt Vector Register (Address: 0x07)

The Interrupt Vector Register (INTVEC) is a byte wide read/write register. An interrupt acknowledge cycle clears the interrupt request and puts the Interrupt Vector onto the data bus.

If interrupts are enabled in the DAC Control Register, interrupts are generated whenever a serial transfer to one of the DACs is finished; i.e. when the DAC_BUSY flag in the DAC Status Register becomes inactive (set to '0').

Bit	Symbol	Description	Access	Reset Value
7:0	INTVEC	Interrupt Vector loaded by software	R/W	0x00

Table 4-5 : Interrupt Vector Register (INTVEC)

4.6 DAC Control Register (Address: 0x0B)

The DAC Control Register (CONTREG) is used to configure interrupts and to set up voltage ranges.

Bit	Symbol	Description	Access	Reset Value
7:3	-	Not used, always read as '0'.	R/W	0
2	INTENA	Interrupt Enable Bit: 1 = Interrupts enabled 0 = Interrupts disabled If interrupts are enabled, interrupts are generated each time the DAC_BUSY flag in the DAC Status Register becomes inactive (set to '0').	R/W	0
1	VRG_2	Voltage Range Selection for DAC Channels 5-8: This Bit has to be configured according to the jumper settings for the output voltage ranges. 1 = ±10V output voltage range and two's complement data coding 0 = 0V to 10V output voltage range and straight binary data coding	R/W	0
0	VRG_1	Voltage Range Selection for DAC Channels 1-4: This Bit has to be configured according to the jumper settings for the output voltage ranges. 1 = ±10V output voltage range and two's complement data coding 0 = 0V to 10V output voltage range and straight binary data coding	R/W	0

Table 4-6 : DAC Control Register (CONTREG)

The VRGx bits in the DAC Control Register select the correct set of ID PROM calibration data values. Therefore, these bits have to be configured prior to reading any calibration data values from the ID PROM and also before starting any data conversion.

5 Functional Description

5.1 DAC Data Coding

Data Value	Analog Output Voltage	
Voltage Range: 0 … 10V (Unipolar)		
0xFFF	+FSR	9.997559V
0x801	Midscale +1LSB	5.002441V
0x800	Midscale	5V
0x7FF	Midscale -1LSB	4.997559V
0x000	-FSR	0V
Voltage Range: -10V … +10V (Bipolar)		
0x7FF	+FSR	+9.995117V
0x001	Midscale +1LSB	+0.0048828V
0x000	Midscale	0V
0xFFF	Midscale -1LSB	-0.0048828V
0x800	-FSR	-10V

Table 5-1 : DAC Data Coding

5.2 Functional State Diagram and Description

An IP_RESET sets the TIP550 into its IDLE state.

After a write access to the DAC Data Register, the TIP550 changes to the DATA_BUSY state and the DATA_BUSY flag in the DAC Status Register is set. In this state, another write access to the DAC Data Register overwrites the current value and the TIP550 remains in the DATA_BUSY state. A write access to the DAC Channel Select Register, however, starts the serial data transfer to the corresponding DAC channel and the TIP550 enters the DAC_BUSY state. The DAC_BUSY flag in the DAC Status Register is set accordingly. As long as the serial transfer is in progress, the DAC_BUSY state is held. If another data value is written into the DAC Data Register during the serial data transfer, the TIP550 enters the DATA_BUSY state again; otherwise it automatically enters the IDLE state when the transfer is finished. The state transition from DAC_BUSY state to IDLE state generates an interrupt if interrupts are enabled in the DAC Control Register.

It is possible to transfer the previously written data value in the DAC Data Register again, when the TIP550 is in IDLE state. In order to do that, a write access to the DAC Channel Select Register has to be performed.

The following state diagram shows the above mentioned principles.

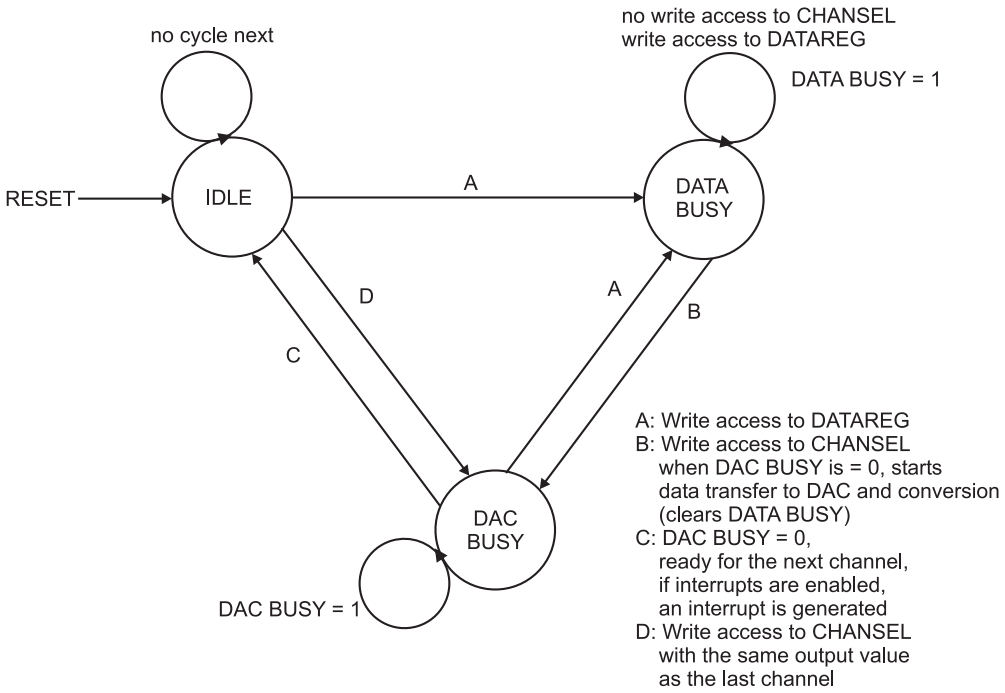

Figure 5-1 : State Diagram of the TIP550 DAC Data Handling

6 Programming Hints

6.1 DAC Data Correction

There are two errors affecting the accuracy of the DAC that can be corrected using the factory calibrated calibration data space.

First, there is the so called “offset error”. For the DAC, this is the data value that is required to produce a zero voltage output signal. This error is corrected by subtracting the offset from the DAC data value.

Second, there is the so called “gain error”. The gain error is the difference between the ideal gain and the actual gain of the DAC. It is corrected by multiplying the DAC data value with a correction factor.

The correction values are obtained during factory calibration and are stored in an on board EEPROM as two’s complement byte-wide values in the range from -128 to +127. To achieve a higher accuracy, they are scaled to ¼LSB.

Because offset and gain correction values are dependent on the selected output voltage range, the TIP550-10 has four different sets of ID PROM data (four combinations of output voltage ranges for the two groups of D/A channels) and the TIP550-11x has two different sets of ID PROM data (two combinations of output voltage ranges for one group of D/A channels).

Before accessing the correction values from the ID PROM, the DAC Control Register has to be set up identically to the output voltage ranges configured by the jumpers.

6.1.1 DAC Value Correction for 0V…10V Output Voltage Range

The basic formula for correction the DAC output value in unipolar mode is:

$$\mathbf{Data = Value * (1 - GAIN_{corr} / 16384) - OFFSET_{corr} / 4}$$

Data is the corrected digital value that should be programmed to the data register. *Value* is the ideal digital value for the desired output voltage. $GAIN_{corr}$ and $OFFSET_{corr}$ are the correction factors from the on board EEPROM. $GAIN_{corr}$ and $OFFSET_{corr}$ are stored separately for each of the possible D/A channels.

6.1.2 DAC Value Correction for ±10V Output Voltage Range

The basic formula for correcting DAC output value in bipolar mode is:

$$\mathbf{Data = Value * (1 - GAIN_{corr} / 8192) - OFFSET_{corr} / 4}$$

Data is the corrected digital value that should be programmed to the data register. *Value* is the ideal digital value for the desired output voltage. $GAIN_{corr}$ and $OFFSET_{corr}$ are the correction factors from the on board EEPROM. $GAIN_{corr}$ and $OFFSET_{corr}$ are stored separately for each of the possible D/A channels.

The $GAIN_{corr}$ and $OFFSET_{corr}$ values can be read in the Calibration Data Space.

Floating point arithmetic or scaled integer arithmetic is necessary to avoid rounding errors while computing the above formulas.

7 Installation

7.1 Jumper Configuration

The TIP550 has to be configured by jumpers for the desired output voltage ranges. For the TIP550, it is possible to select different output voltage ranges for a group of four channels. Channels 1-4 and channels 5-8 are grouped together. The following table shows the corresponding jumper settings.

	TIP550-10/-11	TIP550-10 only
Voltage Range	**Group 1 (Channels 1-4)**	**Group 2 (Channels 5-8)**
0V…10V	J1, J2: 1-2 installed	J3, J4: 1-2 installed
±10V	J1, J2: 2-3 installed	J3, J4: 2-3 installed

Table 7-1 : Jumper Configuration for Output Voltage Ranges

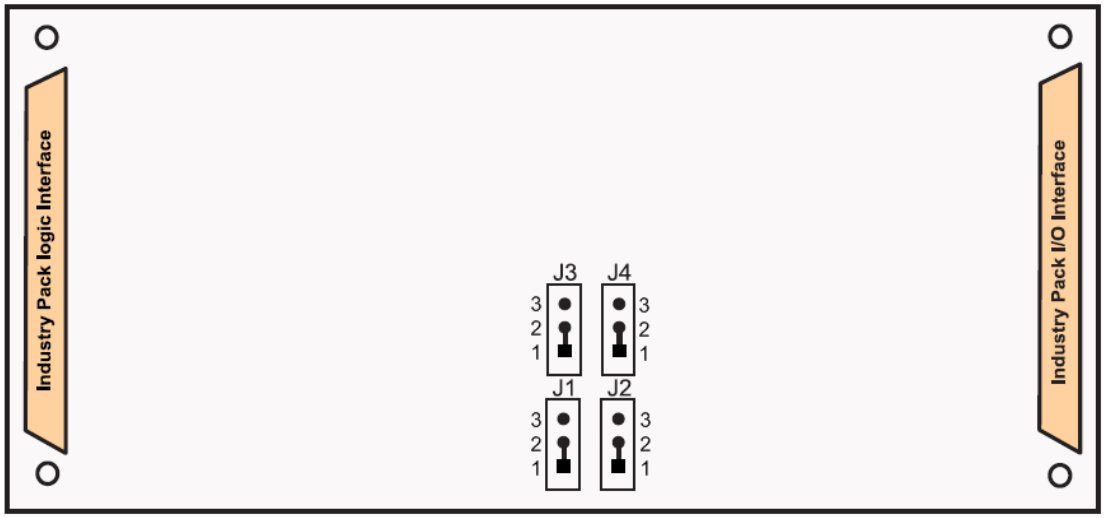

Table 7-2 : Jumper Configuration for Output Voltage Ranges

Factory configuration is 0V…10V for all channels (Jumpers installed on 1-2).

The VRGx bits in the DAC Control Register select the correct set of ID PROM calibration data values. Therefore, these bits have to be configured prior to reading any calibration data values from the ID PROM and also before starting any data conversion.

8 Pin Assignment – I/O Connector

8.1 Pin Assignment

Pin	Signal	
1	DAC Output 1	
2	AGND	
3	DAC Output 2	
4	AGND	
5	DAC Output 3	
6	AGND	
7	DAC Output 4	
8	AGND	
9	DAC Output 5	TIP550-10 only
10	AGND	
11	DAC Output 6	TIP550-10 only
12	AGND	
13	DAC Output 7	TIP550-10 only
14	AGND	
15	DAC Output 8	TIP550-10 only
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		

Pin	Signal	
26		
27		
28		
29		
30		
31		
32		
33		
34		
35		
36		
37		
38		
39		
40		
41		
42		
43		
44	AGND	See Note below
45	-15V	See Note below
46	AGND	See Note below
47	+15V	See Note below
48	AGND	See Note below
49	+5V	See Note below
50	AGND	See Note below

Table 8-1 : Pin Assignment I/O Connector

The Power input connections (Pins 44 to 50) are reserved for special versions of the TIP550 without on board DC/DC converters.

8.2 Connector Orientation

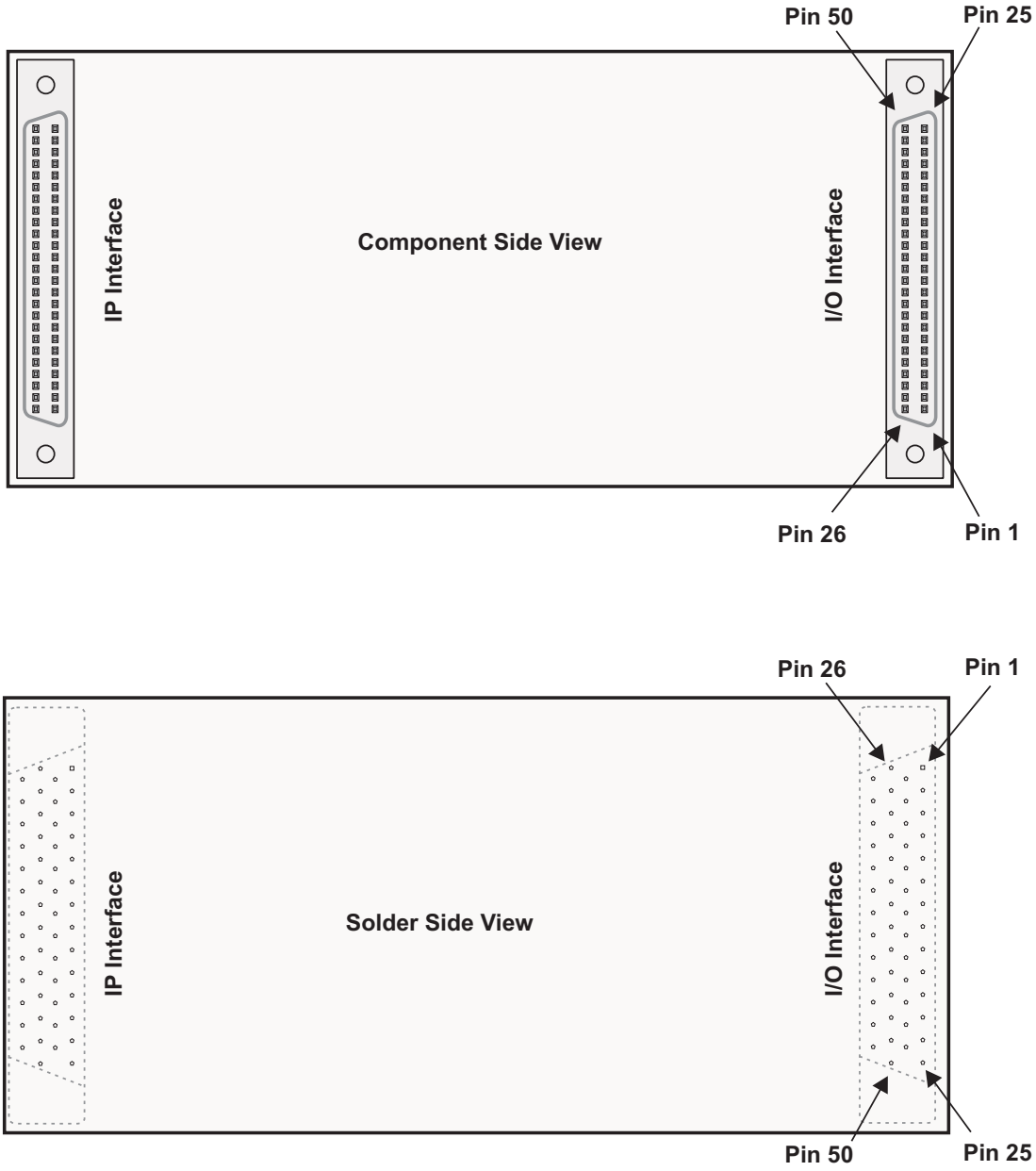

Figure 8-1 : IP Connector Orientation