The Embedded I/O Company

TEWS TECHNOLOGIES

TIP630

Reconfigurable FPGA Digital I/O

Version 1.0

User Manual

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TIP630-10

Reconfigurable FPGA Digital I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, a ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	September 2003
1.1	Modifications chapter “IP Addressing”	November 2003
1.2	New address TEWS LLC	September 2006

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1 Product Description

The TIP630 is an IndustryPack® compatible module providing a user configurable FPGA which controls 48 digital TTL tri-state I/O lines with pull up resistors. The FPGA can be programmed over the IP bus or alternatively by a PROM mounted in a socket. The configuration download is implemented by a pre-programmed CPLD. After the FPGA has initialized, it accesses the IP bus over its own IP interface and the CPLD is only used for reprogramming. The ID space of the CPLD can stay active after configuring the FPGA or it can be switched off and be replaced by an ID ROM implemented in the FPGA.

8 MHz and 32 MHz IP clock is supported by the logic. A 32 MHz oscillator is on board and a PLL clock generator provides two programmable clocks which are programmed through the CPLD.

All control signals of the IP interface are routed to the FPGA. A VHDL example for the FPGA is provided, the design software *ISE WebPACK*, to compile own designs, can be downloaded free of charge at the Xilinx Website (www.xilinx.com).

6 resistor networks mounted in sockets are used to pull the tri-state I/O lines to a logic high value. The resistor networks can be removed or changed in value.

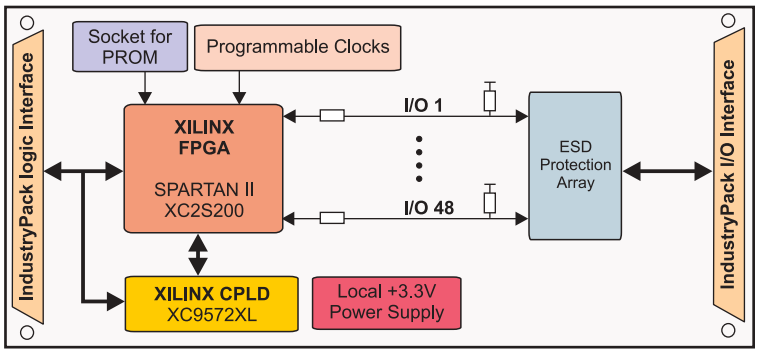

Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used	
Memory Space	Not used in CPLD, possible for FPGA	
Interrupts	Int1 / Int2 not used by CPLD, possible for FPGA	
DMA	Not supported by CPLD, possible for FPGA	
Clock Rate	8MHz / 32MHz	
Module Type	Type I	
Wait States	CPLD: FPGA:	1 wait state for I/O and ID reads no wait states for I/O write depending on design
On Board Devices		
CPLD	Xilinx XC9572XL-10-TQ100-I	
FPGA	Xilinx XC2S200-5-FG256-I	
Clock Generator	Cypress CY22150FI	
I/O Interface		
Interface Connector	50-conductor flat cable	
Number of TTL I/O Lines	48 lines	
Termination	4.7k ohms resistor network as pull up for each tri-state I/O line, changeable and removable in groups of eight resistors	
Output 'Low' Current	–12mA maximum	
Output 'High' Current	Limited by 4k7 pull up to 1mA	
On Board Clock Frequencies	Programmable 250kHz .. 166MHz	
Physical Data		
Power Requirements	130mA typical @ +5V DC, FPGA not configured 110mA typical @ +5V DC, configured with example design	
Temperature Range	Operating Storage	-40°C to +85°C -65°C to +125°C
MTBF	526.000h	
Humidity	5 – 95 % non-condensing	
Weight	30g	

Figure 2-1 : Technical Specification

3 ID PROM Content

Address	Function	Contents
0x01	ASCII 'I'	**0x49**
0x03	ASCII 'P'	**0x50**
0x05	ASCII 'A'	**0x41**
0x07	ASCII 'H'	**0x48**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x38**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0C**
0x17	CRC	**0xEB**
0x19	Version	**0x0D**

Figure 3-1 : ID PROM Content in CPLD

The ID PROM content in the FPGA can be changed by modifying the VHDL source (see chapter "FPGA Example Design / ID PROM Content")

4 IP Addressing

4.1 I/O Addressing

The I/O space of the TIP630 is shared by the FPGA and the CPLD:

Device	Address Range
Spartan II FPGA	0 .. 0x7B
XC9500XL CPLD	0x7C .. 0x7F

Figure 4-1 : I/O Space Registers / word access

The TIP630 CPLD is accessed in the I/O space through the following set of direct accessible registers. All registers can be read/written by word (16 bit) or byte (8 bit) accesses.

4.1.1 Access to TIP630 CPLD Registers

Register Name	Register Symbol	Size	Address
Configuration Register	CONF_REG	16 bit	0x7C
Program Register	PROG_REG	16 bit	0x7E

Figure 4-2 : I/O Space Registers

4.2 Configuration Register

The Configuration Register is a 16 bit wide read/write register used by the main part of the download procedure.

Bit Number	Bit Symbol	Description	Access
15 (MSB)	Spartan_D7	Data byte for Slave Parallel configuration of the FPGA	R/W
14	Spartan_D6		
13	Spartan_D5		
12	Spartan_D4		
11	Spartan_D3		
10	Spartan_D2		
9	Spartan_D1		
8	Spartan_D0		
7	-	Reserved (0 for reads)	-
6	-		
5	-		
4	-		
3	-		
2	-		
1	-		
0 (LSB)	Spartan_CCLK	Configuration Clock for FPGA	R/W

Figure 4-3 : Configuration Register / word access (IP Base Address + 0x7C)

After power-on and reset all outputs, controlled by the Configuration Register, are set to tri-state.

4.3 Program Register

The Program Register is a byte wide read/write register. SCLK and SDAT are used for programming the on board clock generator. The other bits are used to control the configuration signals before and after downloading.

Bit Number	Bit Symbol	Description	Access
15 (MSB)	-	Reserved (0 for reads)	-
14	-	Reserved (0 for reads)	-
13	-	Reserved (0 for reads)	-
12	-	Reserved (0 for reads)	-
11	-	Reserved (0 for reads)	-
10	-	Reserved (0 for reads)	-
9	-	Reserved (0 for reads)	-
8	-	Reserved (0 for reads)	-
7	SCLK	Clock Generator SCLK	R/W
6	SDAT	Clock Generator SDAT	R/W
5	-	Reserved (0 for reads)	-
4	Spartan_INIT	Configuration INIT	R
3	Spartan_DONE	Configuration DONE	R
2	Spartan_CSN	Configuration CS	R/W
1	Spartan_WRN	Configuration WRITE	R/W
0 (LSB)	Spartan_PROG_OE	Configuration PROGRAM OE 0: Tristate 1: Pull PROGRAM Low (force reconfiguration)	R/W

Figure 4-4 : Program Register (IP Base Address + 0x7E)

After power-on and reset SCLK and SDAT are '1', all other outputs are set to tri-state.

4.3.1 Clock Programming

The CY22150 is programmed over a serial 2-wire programming interface with the serial clock signal SCLK and the serial data signal SDAT. The CY22150 is addressed as a slave device on the 2-wire bus with an address of 0x69. A detailed register description and the exact programming timing can be found in the datasheet of the CY22150. This is available from www.cypress.com, together with the program 'CyberClocks', which helps calculating the register values.

5 FPGA Programming Hints

5.1 FPGA Design

As already mentioned, own FPGA designs can be developed using the *ISE WebPACK*, which can be downloaded free of charge at the Xilinx Website (www.xilinx.com). Taking the VHDL example provided with the Engineering Manual would be a good basis. After synthesizing the logic, the resulting `.rbt` file has to be converted to a hex format which can be downloaded by the driver. This conversion can be done by the Xilinx PROMGen program. To give the user more comfort, Xilinx has published a perl script with the application note xapp502 that does the necessary formatting. To run the script, perl 5 must be installed, e.g. the free ActivePerl from www.activestate.com/Products/ActivePerl.

5.2 FPGA Pin Assignment

5.2.1 Pin Assignment of FPGA I/O Lines

Signal	Pin	Signal	Pin
IO47	B16	IO23	F16
IO46	C16	IO22	G14
IO45	D16	IO21	G15
IO44	E15	IO20	H15
IO43	J14	IO19	M15
IO42	K15	IO18	P16
IO41	L16	IO17	R16
IO40	L15	IO16	T15
IO39	T14	IO15	T11
IO38	T13	IO14	T10
IO37	R13	IO13	R10
IO36	R12	IO12	T9
IO35	T8	IO11	T6
IO34	T7	IO10	T5
IO33	R7	IO9	T3
IO32	R6	IO8	T2
IO31	R1	IO7	L1
IO30	P1	IO6	K1
IO29	N2	IO5	J1
IO28	M1	IO4	H1
IO27	G2	IO3	E2
IO26	F1	IO2	D2
IO25	F2	IO1	C2
IO24	E1	IO0	B1

Figure 5-1 : Pin Assignment FPGA I/O Lines

5.2.2 Pin Assignment of IP Bus Signals

Signal	Pin	Signal	Pin
D15	A11	R_W#	A2
D14	B11	RESET#	E4
D13	B10	IOSEL#	C7
D12	D10	INTSEL#	D6
D11	A9	IDSEL#	D5
D10	A8	MEMSEL#	E3
D9	C8	INTREQ0#	A10
D8	A7	INTREQ1#	B9
D7	D7	BS1#	A12
D6	A6	BS0#	C12
D5	B6	ACK#	A14
D4	A5	CLK	B8
D3	C5	DMAREQ0#	B4
D2	A4	DMAREQ1#	B5
D1	A3	DMACK0#	E6
D0	B3	DMAEND#	M3
A6	A13	STROBE#	E14
A5	B12		
A4	D11		
A3	C10		
A2	D9		
A1	D8		

Figure 5-2 : Pin Assignment IP Bus Signals

5.2.3 Pin Assignment of Auxiliary Clock Signals

CLK32	C9
EX_CLK1	N8
EX_CLK2	R8

Figure 5-3 : Pin Assignment Clock Inputs

5.2.4 Pin Assignment of other Signals

ID_ENA	G4
reserved	F3
reserved	F4

Figure 5-4 : Pin Assignment of other Signals

5.3 FPGA Example Design

The FPGA Example VHDL code supports register access to the 48 digital I/O lines.

The line inputs are always enabled; this allows determining the state of the I/O line at any time. It can be used as read back function for lines configured as outputs. The direction register is used to set each I/O line separately as input or output. After power-on or reset all I/O lines are configured as inputs.

The FPGA example design is only tested with 8MHz IP clock speed.

To reduce the cross talk on the TIP630 not all 48 I/O lines are switched at the same time. The output lines are switched in 8 groups of 6 signals in steps of 15ns. So after about 120ns the switching process is completed.

5.3.1 ID PROM Content

For the ID PROM Content of the FPGA Example see chapter **"ID PROM Content".** The ID PROM content in the FPGA can be changed by modifying the VHDL source. To disable the CPLD ID PROM, the FPGA has to pull the ID_ENA line to low:

```
ID_ENA <= '0';
```

Please be careful when changing manufacturer and model ID of the ID PROM. The operating system should be able to handle the case that these values change after configuration of the FPGA.

5.3.2 IP Bus Address Map

The TIP630 is accessed in the I/O space though the following set of direct accessible registers.

All registers of the TIP630 can be read/written by word (16 bit) or byte (8 bit) accesses.

5.3.2.1 Word Access to FPGA Example Registers

Register Name	I/O lines	Register Symbol	Size	Address
Line Output Register	1 – 16 17 – 32 33 – 48	OUT_REG	16 bit 16 bit 16 bit	0x00 0x02 0x04
Line Input Register	1 – 16 17 – 32 33 – 48	IN_REG	16 bit 16 bit 16 bit	0x06 0x08 0x0A
Line Direction Register	1 – 16 17 – 32 33 – 48	DIR_REG	16 bit 16 bit 16 bit	0x0C 0x0E 0x10

Figure 5-5 : I/O Space Registers / word access

5.3.2.2 Byte Access to FPGA Example Registers

Register Name	I/O lines	Register Symbol	Size	Address
Line Output Register	9 – 16 1 – 8 25 – 32 17 – 24 41 – 48 33 – 40	OUT_REG	8 bit 8 bit 8 bit 8 bit 8 bit 8 bit	0x00 0x01 0x02 0x03 0x04 0x05
Line Input Register	9 – 16 1 – 8 25 – 32 17 – 24 41 – 48 33 – 40	IN_REG	8 bit 8 bit 8 bit 8 bit 8 bit 8 bit	0x06 0x07 0x08 0x09 0x0A 0x0B
Line Direction Register	9 – 16 1 – 8 25 – 32 17 – 24 41 – 48 33 – 40	DIR_REG	8 bit 8 bit 8 bit 8 bit 8 bit 8 bit	0x0C 0x0D 0x0E 0x0F 0x10 0x11

Figure 5-6 : I/O Space Registers / byte access

5.3.3 FPGA Register Description

5.3.3.1 Line Output Register

The Line Output Register is subdivided into three word wide read/write registers. The status of the digital output channels can be set or reset directly by writing to the Line Output Register.

Bit Number	0x00	0x02	0x04	Description	Access
15 (MSB)	OUTPUT 16	OUTPUT 32	OUTPUT 48	To set an output channel active that means set to tri-state level, write '1' to the corresponding bit. For the inactive state write '0' to the corresponding bit. 0 : inactive 1 : active / tri-state	R/W
14	OUTPUT 15	OUTPUT 31	OUTPUT 47		
13	OUTPUT 14	OUTPUT 30	OUTPUT 46		
12	OUTPUT 13	OUTPUT 29	OUTPUT 45		
11	OUTPUT 12	OUTPUT 28	OUTPUT 44		
10	OUTPUT 11	OUTPUT 27	OUTPUT 43		
9	OUTPUT 10	OUTPUT 26	OUTPUT 42		
8	OUTPUT 9	OUTPUT 25	OUTPUT 41		
7	OUTPUT 8	OUTPUT 24	OUTPUT 40		
6	OUTPUT 7	OUTPUT 23	OUTPUT 39		
5	OUTPUT 6	OUTPUT 22	OUTPUT 38		
4	OUTPUT 5	OUTPUT 21	OUTPUT 37		
3	OUTPUT 4	OUTPUT 20	OUTPUT 36		
2	OUTPUT 3	OUTPUT 19	OUTPUT 35		
1	OUTPUT 2	OUTPUT 18	OUTPUT 34		
0 (LSB)	OUTPUT 1	OUTPUT 17	OUTPUT 33		

Figure 5-7 : Line Output Register / word access (IP Base Address + 0x00 / 0x02 / 0x04)

After power-on and reset all bits of Line Output Register are set to active / tri-state value.

Bit Number	0x00	0x01	0x02	Description	Access
7 (MSB)	OUTPUT 16	OUTPUT 8	OUTPUT 32	To set an output channel active that means set to tri-state level, write '1' to the corresponding bit. For the inactive state write '0' to the corresponding bit. 0 : inactive 1 : active / tri-state	R/W
6	OUTPUT 15	OUTPUT 7	OUTPUT 31		
5	OUTPUT 14	OUTPUT 6	OUTPUT 30		
4	OUTPUT 13	OUTPUT 5	OUTPUT 29		
3	OUTPUT 12	OUTPUT 4	OUTPUT 28		
2	OUTPUT 11	OUTPUT 3	OUTPUT 27		
1	OUTPUT 10	OUTPUT 2	OUTPUT 26		
0 (LSB)	OUTPUT 9	OUTPUT 1	OUTPUT 25		

Figure 5-8 : Line Output Register Part 1 / byte access (IP Base Address + 0x00 / 0x01 / 0x02)

Bit Number	0x03	0x04	0x05	Description	Access
7 (MSB)	OUTPUT 24	OUTPUT 48	OUTPUT 40	To set an output channel active that means set to tri-state level, write '1' to the corresponding bit. For the inactive state write '0' to the corresponding bit. 0 : inactive 1 : active / tri-state	R/W
6	OUTPUT 23	OUTPUT 47	OUTPUT 39		
5	OUTPUT 22	OUTPUT 46	OUTPUT 38		
4	OUTPUT 21	OUTPUT 45	OUTPUT 37		
3	OUTPUT 20	OUTPUT 44	OUTPUT 36		
2	OUTPUT 19	OUTPUT 43	OUTPUT 35		
1	OUTPUT 18	OUTPUT 42	OUTPUT 34		
0 (LSB)	OUTPUT 17	OUTPUT 41	OUTPUT 33		

Figure 5-9 : Line Output Register Part 2 / byte access (IP Base Address + 0x03 / 0x04 / 0x05)

Normally the output line is loaded with Line Output Register value direct after IP write access. This process is controlled by the 8MHz IP clock.

To set a TTL line as output, the corresponding bit in the Line Direction Register must be set to '1'.

5.3.3.2 Line Input Register

The Line Input Register is subdivided into three word wide read only registers that reflect the actual state of all 48 digital TTL I/O lines.

Bit Number	0x06	0x08	0x0A	Description	Access
15 (MSB)	INPUT 16	INPUT 32	INPUT 48	0 : TTL I/O line logic low 1 : TTL I/O line logic high	R
14	INPUT 15	INPUT 31	INPUT 47		
13	INPUT 14	INPUT 30	INPUT 46		
12	INPUT 13	INPUT 29	INPUT 45		
11	INPUT 12	INPUT 28	INPUT 44		
10	INPUT 11	INPUT 27	INPUT 43		
9	INPUT 10	INPUT 26	INPUT 42		
8	INPUT 9	INPUT 25	INPUT 41		
7	INPUT 8	INPUT 24	INPUT 40		
6	INPUT 7	INPUT 23	INPUT 39		
5	INPUT 6	INPUT 22	INPUT 38		
4	INPUT 5	INPUT 21	INPUT 37		
3	INPUT 4	INPUT 20	INPUT 36		
2	INPUT 3	INPUT 19	INPUT 35		
1	INPUT 2	INPUT 18	INPUT 34		
0 (LSB)	INPUT 1	INPUT 17	INPUT 33		

Figure 5-10 : Line Input Register / word access (IP Base Address + 0x06 / 0x08 / 0x0A)

Bit Number	0x00	0x01	0x02	Description	Access
7 (MSB)	INPUT 16	INPUT 8	INPUT 32	0 : TTL I/O line logic low 1 : TTL I/O line logic high	R
6	INPUT 15	INPUT 7	INPUT 31		
5	INPUT 14	INPUT 6	INPUT 30		
4	INPUT 13	INPUT 5	INPUT 29		
3	INPUT 12	INPUT 4	INPUT 28		
2	INPUT 11	INPUT 3	INPUT 27		
1	INPUT 10	INPUT 2	INPUT 26		
0 (LSB)	INPUT 9	INPUT 1	INPUT 25		

Figure 5-11 : Line Input Register Part 1 / byte access (IP Base Address + 0x06 / 0x07 / 0x08)

Bit Number	0x03	0x04	0x05	Description	Access
7 (MSB)	INPUT 24	INPUT 48	INPUT 40	0 : TTL I/O line logic low 1 : TTL I/O line logic high	R
6	INPUT 23	INPUT 47	INPUT 39		
5	INPUT 22	INPUT 46	INPUT 38		
4	INPUT 21	INPUT 45	INPUT 37		
3	INPUT 20	INPUT 44	INPUT 36		
2	INPUT 19	INPUT 43	INPUT 35		
1	INPUT 18	INPUT 42	INPUT 34		
0 (LSB)	INPUT 17	INPUT 41	INPUT 33		

Figure 5-12 : Line Input Register Part 2 / byte access (IP Base Address + 0x09 / 0x0A / 0x0B)

Normally the input lines are latched into Line Input Register every rising edge of the IP 8MHz clock.

5.3.3.3 Line Direction Register

The Line Direction Register is subdivided into three word read/write registers. To enable the output lines the corresponding bit of the Line Direction Register must be set to logic level '1'. To disable the output lines and switch to an 'input only' line the logic level '0' has to be written into the Line Direction Register.

Bit Number	0x0C	0x0E	0x10	Description	Access
15 (MSB)	DIR 16	DIR 32	DIR 48	0 : TTL I/O line is Input 1 : TTL I/O line is Output	R/W
14	DIR 15	DIR 31	DIR 47		
13	DIR 14	DIR 30	DIR 46		
12	DIR 13	DIR 29	DIR 45		
11	DIR 12	DIR 28	DIR 44		
10	DIR 11	DIR 27	DIR 43		
9	DIR 10	DIR 26	DIR 42		
8	DIR 9	DIR 25	DIR 41		
7	DIR 8	DIR 24	DIR 40		
6	DIR 7	DIR 23	DIR 39		
5	DIR 6	DIR 22	DIR 38		
4	DIR 5	DIR 21	DIR 37		
3	DIR 4	DIR 20	DIR 36		
2	DIR 3	DIR 19	DIR 35		
1	DIR 2	DIR 18	DIR 34		
0 (LSB)	DIR 1	DIR 17	DIR 33		

Figure 5-13 : Line Direction Register / word access (IP Base Address + 0x0C / 0x0E / 0x10)

Bit Number	0x00	0x01	0x02	Description	Access
7 (MSB)	INPUT 16	DIR 8	DIR 32	0 : TTL I/O line is Input 1 : TTL I/O line is Output	R/W
6	DIR 15	DIR 7	DIR 31		
5	DIR 14	DIR 6	DIR 30		
4	DIR 13	DIR 5	DIR 29		
3	DIR 12	DIR 4	DIR 28		
2	DIR 11	DIR 3	DIR 27		
1	DIR 10	DIR 2	DIR 26		
0 (LSB)	DIR 9	DIR 1	DIR 25		

Figure 5-14 : Line Direction Register Part 1 / byte access (IP Base Address + 0x0C / 0x0D / 0x0E)

Bit Number	0x03	0x04	0x05	Description	Access
7 (MSB)	DIR 24	DIR 48	DIR 40	0 : TTL I/O line is Input 1 : TTL I/O line is Output	R/W
6	DIR 23	DIR 47	DIR 39		
5	DIR 22	DIR 46	DIR 38		
4	DIR 21	DIR 45	DIR 37		
3	DIR 20	DIR 44	DIR 36		
2	DIR 19	DIR 43	DIR 35		
1	DIR 18	DIR 42	DIR 34		
0 (LSB)	DIR 17	DIR 41	DIR 33		

Figure 5-15 : Line Direction Register Part 2 / byte access (IP Base Address + 0x0F / 0x10 / 0x11)

The reset value of the Line Direction Register is 0x0000 0000 0000. That means all TTL output lines are disabled.

6 Installation

6.1 Pull Up Resistors

Six resistor networks (8 x 4.7k ohms) mounted in sockets are used to pull up the tri-state TTL I/O lines. The resistor networks can be removed or changed in value.

A resistor network is made out of eight individual resistors in one serial package.

Groups of resistors:

N19 : I/O line 1 – 8

N18 : I/O line 25 – 32

N17 : I/O line 9 – 16

N16 : I/O line 33 – 40

N15 : I/O line 17 – 24

N14 : I/O line 41 – 48

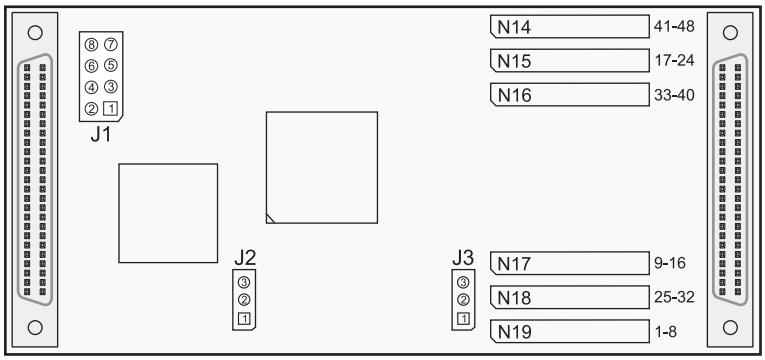

Figure 6-1 : Location of Pull Up Resistors

Resistor pining:

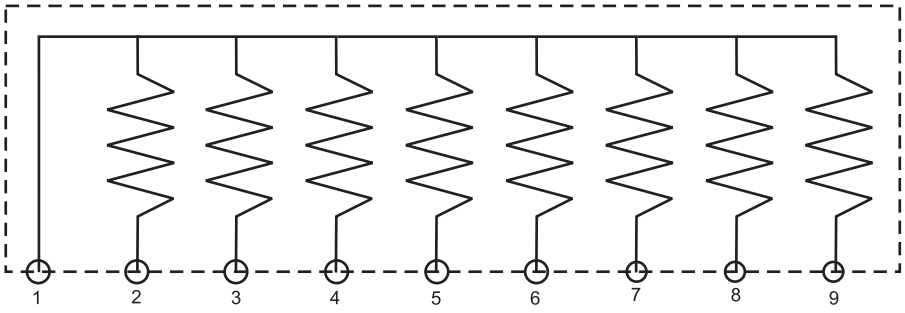

Figure 6-2 : Pining of Pull Up Resistors

6.2 Configuration Source

To select between the IP bus and the on board PROM as the source for the configuration of the FPGA, use jumper J2. Default setting is configuration over the IP interface.

Jumper J2 1 – 2 : configuration over IP bus (default)

Jumper J2 2 – 3 : configuration by PROM

To configure the FPGA by PROM, mount a programmed Xilinx XC17S200APD8I to the Socket. Caution: Never put J2 in position 2-3 (IP bus) when a PROM is mounted.

6.3 Pull Up Voltage

To fit the maximum I/O output voltage to 5V or alternative 3.3V for designs with only 3.3V tolerant devices use the jumper J3. The default is 5V I/O voltage.

Jumper J3 1 – 2 : I/O Voltage 3.3V

Jumper J3 2 – 3 : I/O Voltage 5V (default)

J1 is not relevant for customers.

6.4 TTL I/O Interface

The 48 TTL I/O lines are realized with an Input / Output Register built in the XILINX FPGA and a few external passive devices. A serial resistor reduces spikes during switching process. The 4.7k ohms pull up for the tri-state output function and an electronic protection array for ESD and overvoltage protection.

See the following figure for more information of electrical circuitry.

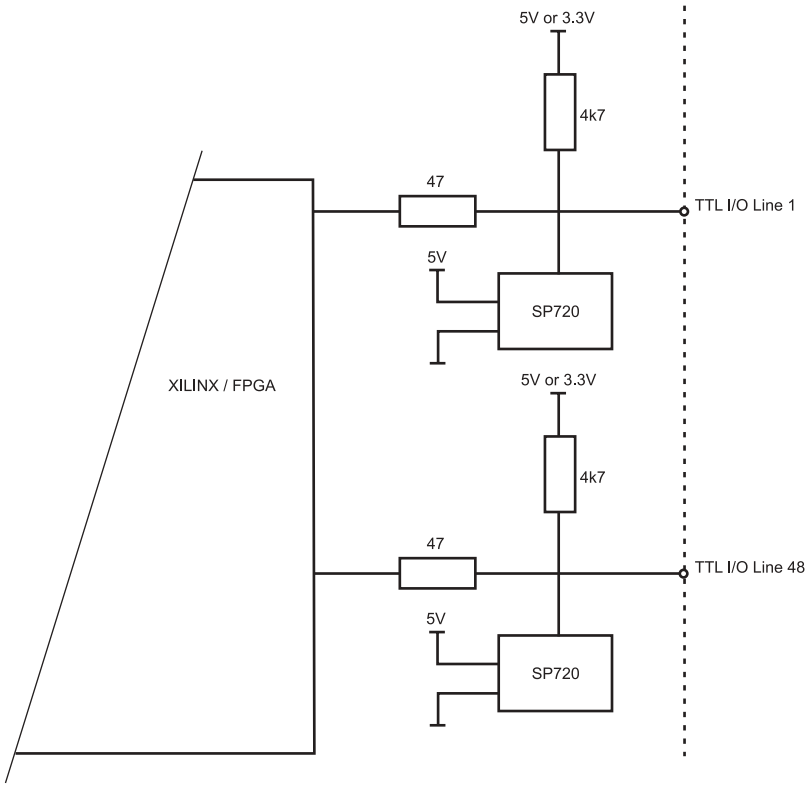

Figure 6-3 : TTL I/O Interface

Please note that the length and with it the large capacitance of flat cable connected to the TIP630 module should be kept very short to prevent large cross talk.

To reduce the cross talk on the TIP630 not all 48 I/O lines should be switched at the same time. The output lines could be switched in 8 groups of 6 signals in steps of 15ns, as shown in the VHDL example. After about 120ns the switching process is completed.

7 Pin Assignment – I/O Connector

Pin	Signal
1	TTL I/O Line 1
2	TTL I/O Line 2
3	TTL I/O Line 3
4	TTL I/O Line 4
5	TTL I/O Line 5
6	TTL I/O Line 6
7	TTL I/O Line 7
8	TTL I/O Line 8
9	TTL I/O Line 9
10	TTL I/O Line 10
11	TTL I/O Line 11
12	TTL I/O Line 12
13	TTL I/O Line 13
14	TTL I/O Line 14
15	TTL I/O Line 15
16	TTL I/O Line 16
17	TTL I/O Line 17
18	TTL I/O Line 18
19	TTL I/O Line 19
20	TTL I/O Line 20
21	TTL I/O Line 21
22	TTL I/O Line 22
23	TTL I/O Line 23
24	TTL I/O Line 24
25	TTL I/O Line 25

Pin	Signal
26	TTL I/O Line 26
27	TTL I/O Line 27
28	TTL I/O Line 28
29	TTL I/O Line 29
30	TTL I/O Line 30
31	TTL I/O Line 31
32	TTL I/O Line 32
33	TTL I/O Line 33
34	TTL I/O Line 34
35	TTL I/O Line 35
36	TTL I/O Line 36
37	TTL I/O Line 37
38	TTL I/O Line 38
39	TTL I/O Line 39
40	TTL I/O Line 40
41	TTL I/O Line 41
42	TTL I/O Line 42
43	TTL I/O Line 43
44	TTL I/O Line 44
45	TTL I/O Line 45
46	TTL I/O Line 46
47	TTL I/O Line 47
48	TTL I/O Line 48
49	Signal Ground
50	Signal Ground

Figure 7-1 : Pin Assignment I/O Connector