The Embedded I/O Company

TEWS TECHNOLOGIES

TIP865

4 Channel Serial IP

Version 1.0

User Manual

Issue 1.0.10

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TIP865-10

4 channel RS232 serial I/O

TIP865-11

4 channel TTL serial I/O

TIP865-20

4 channel RS422 serial I/O

TIP865-30

4 channel RS485 serial I/O

TIP865-51

2 channel RS485 serial I/O

2 channel RS422 serial I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	June 1994
1.1	TIP865-30 added	September 1994
1.2	TIP865-51 added	October 2000
1.3	Add Interrupt Routing Description	August 2002
1.4	Addition “Technical Specification”	April 2003
1.5	Correction Baud Rate Value of TIP865-30	July 2003
1.6	Addition Maximum Baud Rates	September 2004
1.7	New address TEWS LLC	September 2006
1.0.8	Fixed a bug in Figure 6-1 and Updated Figures 1-1, 6-4 up to 6-6	December 2008
1.0.9	Addition “Technical Specification”	March 2009
1.0.10	Structural Document Revise	August 2010

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1 Product Description

The TIP865 provides four channels of a high performance multi-mode serial interface. Five different versions are available. The TIP865-10 offers four RS232 interfaces, the TIP865-11 provides four TTL interfaces, the TIP865-20 supports four RS422 interfaces, the TIP865-30 provides four RS485 multidrop interfaces, and the TIP865-51 offers two RS422 and two RS485 interfaces.

Full modem control is available for each of the 4 serial interfaces on the TIP865-10 and –11 supporting RxD, TxD, RTS, CTS, DCD and clock. The TIP865-20 provides RxD, TxD and clock. The TIP865-30 supports a bi-directional RS485 bus. The baud rate is individually programmable up to 2 Mbaud.

The TIP865-51 is a combination of the TIP865-20 and –30. Two channels support RxD, TxD and clock for the RS422 interface and two channels supports a bi-directional RS485 bus.

Features include programmable baud rates to 2 Mbit/sec, asynchronous or synchronous protocols including NRZ, NRZI, FM, T1, SDLC/HDLC.

The communication controller used is the industry standard Z85C30.

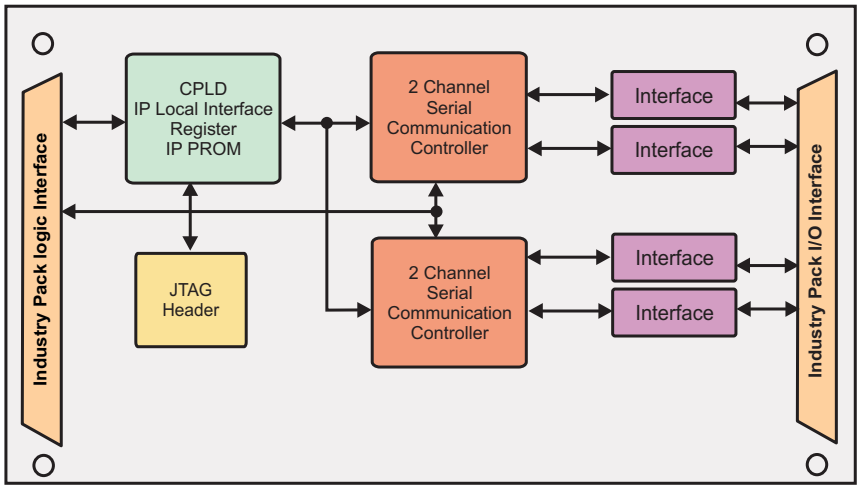

Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I Access: no wait states	
I/O Space	Access: 1 wait state	
Memory Space	Not used	
Interrupts	Vectored interrupts, IntReq0 and IntReq1 used Access: 2 wait states	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
On Board Devices		
Serial Communication Controller	Zilog Z85C3016PSC	
I/O Interface		
Interface Connector	50-conductor flat cable	
Termination	TIP865-10: no termination TIP865-11: no termination TIP865-20: supports receive and transmit termination TIP865-30: a standard RS485 termination available TIP865-51: supports receive termination for RS422 inputs and a standard RS485 termination for the RS485 channels	
I/O Signals	TIP865-10 (RS232): TxD, RTS, DTR, RxD, CTS, DSR, DCD, clock (in and out) TIP865-11 (TTL): TxD, RTS, DTR, RxD, CTS, DSR, DCD, clock (in and out) TIP865-20 (RS422): TxD, RxD, CLKIN, CLKOUT TIP865-30 (RS485): TxD/RxD+, TxD/RxD- TIP865-51 (RS422/RS485): TxD, RxD, CLKIN, CLKOUT resp. TxD/RxD+, TxD/RxD-	
Power Requirements	120mA typical @ +5V DC (measured with I/O pins open)	
Physical Data		
Temperature Range	Operating Storage	0 °C to +70 °C -40°C to +125°C

MTBF	TIP865-10: 1427000h TIP865-11: 1518000h TIP865-20: 1475000h TIP865-30: 920000h TIP865-51: 732000h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	TIP865-10: 46g TIP865-11: 42g TIP865-20: 45g TIP865-30: 45g TIP865-51: 46g

Table 2-1 : Technical Specification

3 ID Prom Contents

Address	Function	TIP865-10	TIP865-11	TIP865-20	TIP865-30	TIP865-51
0x01	ASCII 'I'	0x49	0x49	0x49	0x49	0x49
0x03	ASCII 'P'	0x50	0x50	0x50	0x50	0x50
0x05	ASCII 'A'	0x41	0x41	0x41	0x41	0x41
0x07	ASCII 'C'	0x43	0x43	0x43	0x43	0x43
0x09	Manufacturer ID	0xB3	0xB3	0xB3	0xB3	0xB3
0x0B	Model Number	0x10	0x10	0x10	0x10	0x10
0x0D	Revision	0x10	0x10	0x10	0x10	0x10
0x0F	RESERVED	0x00	0x00	0x00	0x00	0x00
0x11	Driver-ID Low - Byte	0x00	0x00	0x00	0x00	0x00
0x13	Driver-ID High - Byte	0x00	0x00	0x00	0x00	0x00
0x15	Number of bytes used	0x10	0x10	0x10	0x10	0x10
0x17	CRC	0x21	0x9D	0x09	0xC4	0x73
0x19	SIO1 : RS232	0x01				
0x1B	SIO2 : RS232	0x01				
0x1D	SIO3 : RS232	0x01				
0x1F	SIO4 : RS232	0x01				
0x19	SIO1 : TTL		0x02			
0x1B	SIO2 : TTL		0x02			
0x1D	SIO3 : TTL		0x02			
0x1F	SIO4 : TTL		0x02			
0x19	SIO1 : RS422			0x03		
0x1B	SIO2 : RS422			0x03		
0x1D	SIO3 : RS422			0x03		
0x1F	SIO4 : RS422			0x03		
0x19	SIO1 : RS485				0x04	
0x1B	SIO2 : RS485				0x04	
0x1D	SIO3 : RS485				0x04	
0x1F	SIO4 : RS485				0x04	
0x19	SIO1 : RS485					0x04
0x1B	SIO2 : RS485					0x04
0x1D	SIO3 : RS422					0x03
0x1F	SIO4 : RS422					0x03

Table 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The TIP865 is accessed in the I/O space through the following set of external registers of two Z85C30 Serial Communication Controllers (SCC).

Address	Name	Function	Size
0x01	CHCON2	Port 2 control register (SCC 1B Control)	byte
0x03	CHDAT2	Port 2 data register (SCC 1B Data)	byte
0x05	CHCON1	Port 1 control register (SCC 1A Control)	byte
0x07	CHDAT1	Port 1 data register (SCC 1A Data)	byte
0x09	CHCON4	Port 4 control register (SCC 2B Control)	byte
0x0B	CHDAT4	Port 4 data register (SCC 2B Data)	byte
0x0D	CHCON3	Port 3 control register (SCC 2A Control)	byte
0x0F	CHDAT3	Port 3 data register (SCC 2A Data)	byte

Table 4-1 : Register Map

For more details of the Z85C30 SCC, its internal registers and its programming see the Z85C30 Data Sheet, which is part of the TIP865-ED Engineering Documentation.

4.2 Memory Addressing

Not used.

4.3 Interrupt Routing

The four serial communication ports of the TIP865 are realized with two Z85C30 Serial Communication Controllers. Each controller has its own Interrupt Request line which is routed direct to one of the IP interface signals INTREQ0 or INTREQ1.

Serial Communication Ports	IP Interrupt
Channel 1	INTREQ0
Channel 2	INTREQ0
Channel 3	INTREQ1
Channel 4	INTREQ1

Table 4-2 : Interrupt Routing

To enable interrupts for all four serial communication ports both serial communication controllers must be interrupt enabled. Also both interrupt request lines from the IP interface must be configured.

5 Programming Hints

Baud rates may be derived from a local 3.6864 MHz oscillator frequency is permitting the generation of all standard baud rates (including 19200, 38400 and 57600 baud) with zero error. Some networks and communication protocols may require a different oscillator frequency. For these applications the oscillator may be replaced or an external clock signal can be used.

Each channel of the Z85C30 SCC can be accessed by two addresses in the IP's I/O address space. However the Z85C30 SCC uses an internal set of fifteen registers for each channel, which can only be accessed indirectly. Please refer to the Z85C30 Data Sheet for writing own drivers. This data sheet is available from Zilog Corporation and from TEWS TECHNOLOGIES GmbH as part of the TIP865-ED Engineering Documentation.

5.1 Using internal baud rates

The local 3.6864 MHz oscillator is connected with the RTxC# pin of all channels of the Z85C30 SCC. This is the standard configuration of feeding the programmable baud rate generator with an input clock. To enable the baud rate generator with the 3.6864 MHz clock, the driver software must set the bits D1, D0 of the SCC's internal register W14 to '01'.

To use the output of the baud rate generator as Transmit Clock and Receive Clock the bits D4, D3 and D6, D5 of the internal register WR11 must be set to '10'.

5.2 Using external clock

The TIP865 can be programmed to receive an external clock signal or to transmit an external clock signal. For both modes the SCC's pin TRxC# pin is used as I/O. It can be programmed to function as clock input or clock output.

Although the TRxC# pin of the Z85C30 SCC can be software configured to function as clock input or as clock output, the TIP865 hardware must be configured by jumpers in the corresponding mode.

Each individual channel can be configured by hardware and software to be the source of an external clock signal or to receive an external clock signal, but not both at the same time.

5.2.1 Receiving an external clock

To use the Z85C30 SCC's TRxC# pin as input for the external clock the bit D2 of internal register WR11 must be set to value '0'. The external clock is used as Transmit Clock if the bits D4, D3 of internal register WR11 are set to '01' and it is used as Receive Clock if the bits D6, D5 are set to '01'.

5.2.2 Transmitting an external clock signal

To use the Z85C30 SCC's TRxC# pin as output for the external clock the bit D2 of internal register WR11 must be set to value '1'. The source of the external clock signal is selected by the state of bits D1, D0 of the internal register WR11.

D1,D0	Clock Source
'00'	3.6864 MHz Oscillator
'01'	Transmit Clock
'10'	Baud Rate Generator Output
'11'	DPPL Output

Table 5-1 : External Clock Source

5.2.3 Overview clock I/O

The different TIP865 interfaces do not make all the same clock I/O functions available.

TTL – interface:

- Direct clock I/O – programmable via SCC register

RS232 – interface:

- Clock I/O direction selectable by jumper for each channel

RS422 – interface:

- Clock I/O direction selectable by jumper for each channel

RS485 – interface:

- Supports no clock I/O

5.3 Baud Rate Configuration

5.3.1 Clock selection

The on board Z85C30 SCC's provides four different clock sources for internal and external use. To select the source an internal write register of the Z85C30 must be used. Different clock sources for receiver and transmitter could be determined. Alternatively the RTxC# pin, the TRxC# pin, the Baud Rate generator output or the DPLL output could be selected.

- All TIP865 use the on board 3.6864MHz quartz oscillator for RTxC# Clock Input. This means for the TIP865-11, -20, -30 and -51 a maximum baud rate of 921.6kbit/sec. The RS232 transceiver of the TIP865-10 limits the baud rate of this interface to 57.6kbit/sec.
- The PCLK pin of the Z85C30 is routed to the 8 MHz IP clock or to the second on board 16 MHz quartz oscillator. The TIP865-10, -11 and -20 are using the 8 MHz. The TIP865-30 and the TIP865-51 are using a second 16 MHz quartz oscillator.
- Like description in chapter 5.2 the TRxC# pin of the Z85C30 could be used as clock input or clock output. If this pin is used for clock input, synchronous baud rates up to 2 Mbit are possible.

  The TIP865-30 and the RS485 interface of the TIP865-51 don't support external clock input or output.

  Additional to select the clock source TRxC# by programming the internal register of the Z85C30 the jumper configuration of TIP865-10, -11, -20 and -51 must be adjusted. For more information about external clock jumper location see chapter "External Clock Jumper Configuration" and "Clock Jumper Configuration".

5.3.2 Maximum Baud Rate

The maximum baud rate of the TIP865 is affected by several options like the clock input source, clock frequency, used clock mode, synchronous or asynchronous serial mode and the on board physical transceiver.

TIP865	**Maximum Baud Rate**		
	RTxC# Input	PCLK Input	Ext. Clock (TRxC#) Input
TIP865-10 RS232	57.6 kbit/sec	100 kbit/sec	100 kbit/sec
TIP865-11 TTL	921.6 kbit/sec	2 Mbit/sec	2 Mbit/sec
TIP865-20 RS422	921.6 kbit/sec	2 Mbit/sec	2 Mbit/sec
TIP865-30 RS485	921.6 kbit/sec	2 Mbit/sec	Clock I/O not supported
TIP865-51 RS485/RS432	921.6 kbit/sec	2 Mbit/sec	2 Mbit/sec Clock I/O not supported for RS485

Table 5-2 : Maximum Baud Rate

For more information of the Z85C30 SCC, clock input switch, clock rate and clock mode see the Z85C30 Data Sheet, which is part of the TIP865-ED Engineering Documentation.

6 Installation

6.1 TIP865-10/-11 and TIP865-20

6.1.1 DSR / DCD Jumper Configuration

The IBM PC compatible DB9 pin layout defines two separate pin for the signals DSR and DCD. However there is only one input at the Z85C30 SCC for this functionality. At the TIP865-10 RS232 IP and the TIP865-11 TTL IP the DSR or DCD can be individually selected for each channel by jumper.

Channel	DSR (jumper installed)	DCD (jumper installed)
1	J32 1—2	J32 2—3
2	J22 1—2	J22 2—3
3	J12 1—2	J12 2—3
4	J42 1—2	J42 2—3

Table 6-1 : DSR/DCD Jumper Table

The TIP865-20 RS422 IP does not provide DSR and DCD. For this version these jumpers are obsolete.

6.1.2 External Clock Jumper Configuration

The TIP865 provides an external clock signal for each channel, which can be programmed individually as external clock output or external clock input. This clock signal is controlled by corresponding TRxCB# pin of the Z85C30 SCC.

At the TIP865-10 RS232 IP and the TIP865-20 RS422 IP the external clock signal must be configured by jumper for input or output.

Channel	Clock out	Clock in
1	J11 close; J10 open	J11 open; J10 close
2	J21 close; J20 open	J21 open; J20 close
3	J31 close; J30 open	J31 open; J30 close
4	J41 close; J40 open	J41 open; J40 close

Table 6-2 : External Clock Jumper Table

The TIP865-11 TTL IP feeds the TRxCB# signal of the Z85C30 SCC directly to the clock I/O pin. For this version these jumpers are obsolete, because the clock signal can be software configured to be a clock input or clock output.

6.1.3 Jumper Location

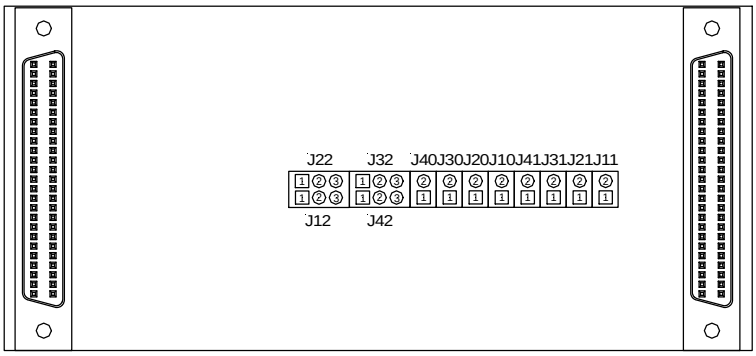

Figure 6-1 : Jumper Location TIP865-10/-11/-20

6.1.4 Termination

The TIP865-10/-11 does not need a termination.

The TIP865-20 RS422 IP supports a standard RS422 termination with termination resistors. Both, receive and transmit termination are available separately for all four serial RS422 channels. A network within all 4 resistors is used to realize the termination. In order to deactivate the termination, the networks must be removed.

Channel	Receive Termination	Transmit Termination
1 + 2	N2 inserted	N1 inserted
3 + 4	N4 inserted	N3 inserted

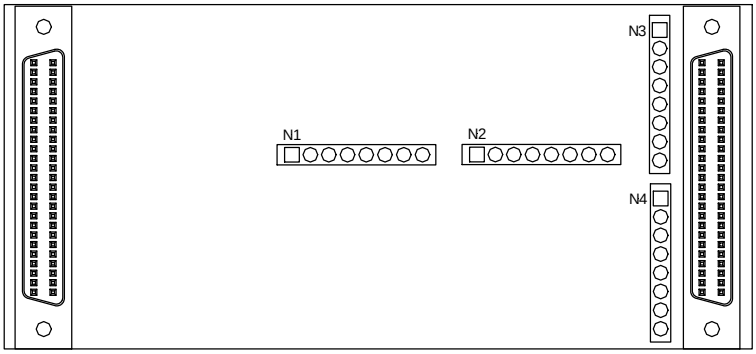

Figure 6-2 : Termination TIP865-20

6.2 TIP865-30

The TIP865-30 supports no clock output or clock input. For this version the jumpers are obsolete. The only signals which build the RS485 interface are the differential RS485+ and RS485- signals.

6.2.1 Termination

A standard serial RS485 termination is intended and selectable. In order to deactivate the termination, the networks must be removed.

Channel	RS485 Termination
1 + 2	N1 inserted
3 + 4	N3 inserted

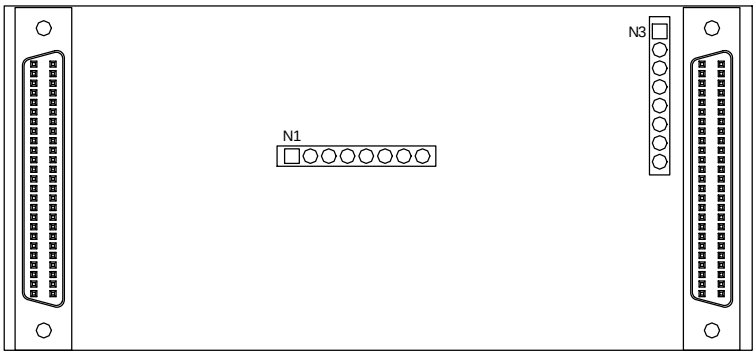

Figure 6-3 : Termination TIP865-30

6.3 TIP865-51

The TIP865-51 is a combination between TIP865-20 and TIP865-30. This version supports two RS485 channels and two RS422 channels.

Just as TIP865-30 the serial interface of the both RS485 channels does not support a clock I/O interface.

6.3.1 Clock Jumper Configuration

The two RS422 channel of the TIP865-51 provide external clock signal, which can be programmed individually as external clock outputs or external clock inputs.

The external clock signal must be configured by jumper for input or output.

Channel	Clock out	Clock in
3	J1 open	J1 close
4	J2 open	J2 close

6.3.2 Termination

The TIP865-51 RS422 channels support a standard RS422 termination. Both, data line (RxD) and clock line (CLKIN) could be terminated. To activate the termination a jumper for each path must be closed and to deactivate the termination the jumper must be removed. A termination for transceiver lines is not supported.

A standard serial RS485 termination is intended for the first two channels of the TIP865-51. To activate the termination the jumper must be closed and to deactivate the termination the jumper must be removed.

Channel	Termination	
	on	**off**
1	J7 close	J7 open
2	J8 close	J8 open
3	J6 close	J6 open
4	J3 close	J3 open
Clock 3	J4 close	J4 open
Clock 4	J5 close	J5 open

6.3.3 Jumper Location

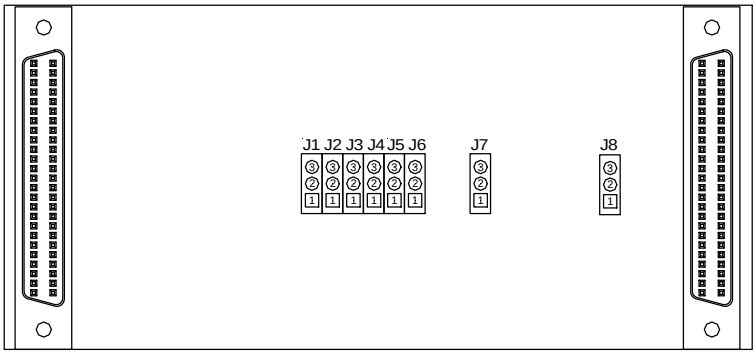

Figure 6-4 : Jumper Location TIP865-51

7 Pin Assignment – I/O Connector

7.1 50 Pin I/O Connector

PIN	TIP865-10/-11	TIP865-20	TIP865-30	TIP865-51
1	DCD 2	TxD+ 2	TxD/RxD+ 2	TxD/RxD+ 2
2	DSR 2	TxD- 2	TxD/RxD- 2	TxD/RxD- 2
3	RxD 2	CLKOUT+ 2		
4	RTS 2	CLKOUT- 2		
5	TxD 2	CLKIN+ 2		
6	CTS 2	CLKIN- 2		
7	DTR 2	RxD+ 2		
8	clock 2	RxD- 2		
9	GND	GND	GND	GND
10	DCD 1	TxD+ 1	TxD/RxD+ 1	TxD/RxD+ 1
11	DSR 1	TxD- 1	TxD/RxD- 1	TxD/RxD- 1
12	RxD 1	CLKOUT+ 1		
13	RTS 1	CLKOUT- 1		
14	TxD 1	CLKIN+ 1		
15	CTS 1	CLKIN- 1		
16	DTR 1	RxD+ 1		
17	clock 1	RxD- 1		
18	GND	GND	GND	GND
19	DCD 4	TxD+ 4	TxD/RxD+ 4	TxD+ 4
20	DSR 4	TxD- 4	TxD/RxD- 4	TxD- 4
21	RxD 4	CLKOUT+ 4		CLKOUT+ 4
22	RTS 4	CLKOUT- 4		CLKOUT- 4
23	TxD 4	CLKIN+ 4		CLKIN+ 4
24	CTS 4	CLKIN- 4		CLKIN- 4
25	DTR 4	RxD+ 4		RxD+ 4
26	clock 4	RxD- 4		RxD- 4
27	GND	GND	GND	GND
28	DCD 3	TxD+ 3	TxD/RxD+ 3	TxD+ 3
29	DSR 3	TxD- 3	TxD/RxD- 3	TxD- 3
30	RxD 3	CLKOUT+ 3		CLKOUT+ 3
31	RTS 3	CLKOUT- 3		CLKOUT- 3
32	TxD 3	CLKIN+ 3		CLKIN+ 3
33	CTS 3	CLKIN- 3		CLKIN- 3
34	DTR 3	RxD+ 3		RxD+ 3
35	clock 3	RxD- 3		RxD- 3
36	GND	GND	GND	GND
37				

PIN	TIP865-10/-11	TIP865-20	TIP865-30	TIP865-51
38				
39				
40				
41				
42				
43				
44	GND	GND	GND	GND
45				
46	GND	GND	GND	GND
47				
48	GND	GND	GND	GND
49	+5V	+5V	+5V	+5V
50	GND	GND	GND	GND

Table 7-1 : Pin Assignment I/O Connector

7.2 DB9 I/O Pin Assignment

The 50 pin flat cable from the IP carrier board may be split into four 9 pin sections, each of these are mass terminated into standard DB9 D-shell connector. For TIP865-10 RS232 module the pin layout is identical with the IBM PC 9 pin connector layout. The only difference is, that pin 9 is not RI signal but used for external clock.

7.2.1 DB9 Pin Assignment: TIP865-10 RS232 and TIP865-11 TTL

PIN	Signal
1	DCD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	clock

Table 7-2 : DB9 Pin Assignment (TIP865-10 RS232 and TIP865-11 TTL)

7.2.2 DB9 Pin Assignment TIP865-20 RS422

PIN	Signal
1	TxD+
2	CLKOUT+
3	CLKIN+
4	RxD+
5	GND
6	TxD-
7	CLKOUT-
8	CLKIN-
9	RxD-

Table 7-3 : DB9 Pin Assignment (TIP865-20 RS422)

7.2.3 DB9 Pin Assignment TIP865-30 RS485

PIN	Signal
1	TxD/RxD+
5	GND
6	TxD/RxD-

Table 7-4 : DB9 Pin Assignment (TIP865-30 RS485)

7.2.4 DB9 Pin Assignment TIP865-51 RS422 and RS485

PIN	Signal – RS422	Signal – RS485
1	TxD+	TxD/RxD+
2	CLKOUT+	
3	CLKIN+	
4	RxD+	
5	GND	GND
6	TxD-	TxD/RxD-
7	CLKOUT-	
8	CLKIN-	
9	RxD-	

Table 7-5 : DB9 Pin Assignment (TIP865-51 RS422 and RS485)

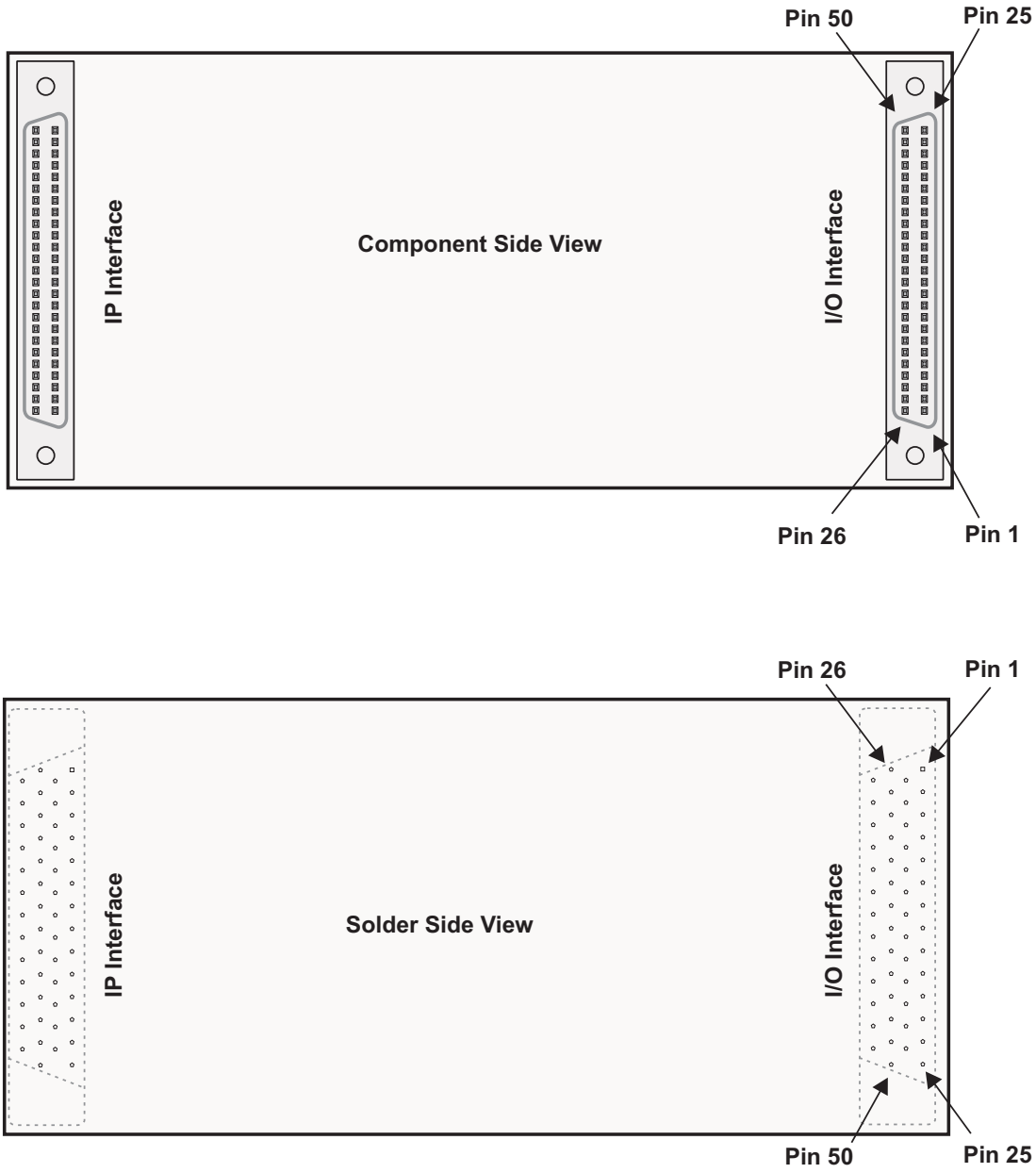

Figure 7-1 : IP Connector Orientation