The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC501

Optically Isolated 32 Channel 16 Bit ADC

Version 1.1

User Manual

Issue 1.1.12

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TPMC501-10
32 single-ended or 16 differential channels of isolated 16 bit ADC, gain 1, 2, 5, 10 input range +/-10V with front panel I/O

TPMC501-11
32 single-ended or 16 differential channels of isolated 16 bit ADC, gain 1, 2, 4, 8 input range +/-10V with front panel I/O

TPMC501-12
32 single-ended or 16 differential channels of isolated 16 bit ADC, gain 1, 2, 5, 10 input range 0V to 10V with front panel I/O

TPMC501-13
32 single-ended or 16 differential channels of isolated 16 bit ADC, gain 1, 2, 4, 8 input range 0V to 10V with front panel I/O

TPMC501-20
32 single-ended or 16 differential channels of isolated 16 bit ADC, gain 1, 2, 5, 10 input range +/-10V with P14 I/O

TPMC501-21
32 single-ended or 16 differential channels of isolated 16 bit ADC, gain 1, 2, 4, 8 input range +/-10V with P14 I/O

TPMC501-22
32 single-ended or 16 differential channels of isolated 16 bit ADC, gain 1, 2, 5, 10 input range 0V to 10V with P14 I/O

TPMC501-23
32 single-ended or 16 differential channels of isolated 16 bit ADC, gain 1, 2, 4, 8 input range 0V to 10V with P14 I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
	Preliminary Issue	January 1999
1.0	First Issue	April 1999
1.1	Revision of Technical Specification	March 2000
1.2	Revision of Interrupt Status Register	June 2000
1.3	Revision of Technical Specification	February 2001
1.4	General Revision	November 2002
1.5	Technical Specification Table corrected	November 2002
1.6	Technical Specification Table corrected	December 2003
1.7	Added note for ADC conversion and Installation Note	October 2004
1.8	New address TEWS LLC	September 2006
1.9	New Hardware Version	April 2008
1.1.10	New notation of User Manual Issue	February 2009
1.1.11	Corrected PCI BAR number in 3.3 Note	October 2009
1.1.12	Added Analog Input Impedance	January 2010

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1 Product Description

The TPMC501 is a PCI Mezzanine Card providing 32 galvanically isolated multiplexed 16 bit ADC channels.

The ADC channels can be software configured to operate in single-ended mode (up to 32 channels) or differential mode (up to 16 channels). Mixed mode configuration is possible.

The analog inputs are overvoltage protected for up to 70 Vpp.

A programmable gain amplifier allows various input voltage ranges.

Board Option	I/O Connection	Gain Factors	Input Voltage Range
TPMC501-10	HD50 Front	1, 2, 5, 10	±10V for gain = 1
TPMC501-11	HD50 Front	1, 2, 4, 8	±10V for gain = 1
TPMC501-12	HD50 Front	1, 2, 5, 10	0V to 10V for gain = 1
TPMC501-13	HD50 Front	1, 2, 4, 8	0V to 10V for gain = 1
TPMC501-20	P14 Back	1, 2, 5, 10	±10V for gain = 1
TPMC501-21	P14 Back	1, 2, 4, 8	±10V for gain = 1
TPMC501-22	P14 Back	1, 2, 5, 10	0V to 10V for gain = 1
TPMC501-23	P14 Back	1, 2, 4, 8	0V to 10V for gain = 1

Table 1-1 : Board Option Overview

Data acquisition and conversion time is mode-dependent. Fastest acquisition and conversion time is 12µs without channel / gain change, 14.5µs with channel / gain change.

The TPMC501 provides a “Sequencer Mode” where the enabled ADC channels can be sampled at a fix rate. For each sequence the ADC data for all enabled channels is stored in a sequencer data RAM.

The repeat frequency of the sequencer can be programmed by using a sequencer timer. The sequencer timer is programmable from 100µs to 6.5535s in steps of 100µs. A special function is the “Sequencer Continuous Mode”. In this mode the sequencer will start a new sequence immediately when a sequence is done.

Each TPMC501 is factory calibrated. The calibration data for each gain is stored in an EEPROM unique to each TPMC501. The modules accuracy is increased by performing data correction in software using the board calibration data values.

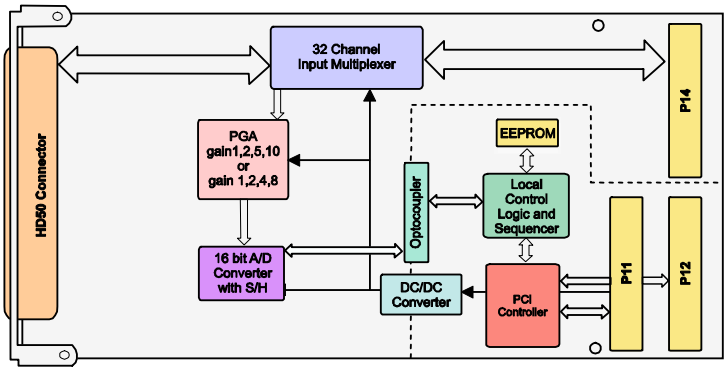

Figure 1-1 : Block Diagram

2 Technical Specification

Logic Interface	
Mechanical Interface	PCI Mezzanine Card Interface (single size)
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	PCI9030 (PLX Technology)
ADC	ADS7809 (Texas Instruments)
PGA	PGA206 / 207 (Texas Instruments)
I/O Interface	
I/O Interface	TPMC501-1x : HD50 female connector (SCSI-2 type) TPMC501-2x : P14 PMC Connector I/O
Number of Analog Channels	32 single-ended channels or 16 differential channels, mixed mode is possible
Input Impedance	Typically 10^{12} Ω (4nA leakage current)
Input Isolation	The analog part (Analog input path and ADC device) is galvanically isolated from the PMC Interface. (1000V isolation voltage)
Input Isolation	The analog part (Analog input path and ADC device) is galvanically isolated from the PMC Interface. (1000V isolation voltage)
Input Gain Amplifier	TPMC501-10 / -20, -12 / -22 : Programmable for gain 1, 2, 5, 10
	TPMC501-11/ -21, -13 / -23 : Programmable for gain 1, 2, 4, 8
Input Voltage Range	TPMC501-10 / -20 : ±10V (gain = 1) ±5V (gain = 2) ±2V (gain = 5) ±1V (gain = 10) TPMC501-11 / -21 : ±10V (gain = 1) ±5V (gain = 2) ±2.5V (gain = 4) ±1.25V (gain = 8)
	TPMC501-12 / -22 : 0V to 10V (gain = 1) 0V to 5V (gain = 2) 0V to 2V (gain = 5) 0V to 1V (gain = 10) TPMC501-13 / -23 : 0V to 10V (gain = 1) 0V to 5V (gain = 2) 0V to 2.5V (gain = 4) 0V to 1.25V (gain = 8)
Input Overvoltage	Protection for up to 70Vpp
Input MUX Leakage Current	typical 4nA
Input PGA Impedance	typical 10^{13} Ohm || 1pF
Input ADC	16 bit ADC

	Data acquisition and conversion time up to 12µs without channel / gain change and up to 14.5µs with channel / gain change (mode-dependent)

Conversion Time with Gain / Channel Change	Normal Mode with Data Pipeline: 14.5µs Normal Mode without Data Pipeline: 22.5µs Automatic Mode with Data Pipeline: 22.5µs Automatic Mode without Data Pipeline: 32.5µs
Calibration Data	Gain and offset factors stored in on board EEPROM
Sequencer	Optional Sequencer Mode 4 bit Instruction RAM for each channel 2x16 bit Data RAM for each channel Continuous Mode : 12µs + 14.5µs per channel Timer Mode : 100µs to 6.5535s (100µs steps)
Accuracy	± 4 LSB after calibration for all TPMC501 modules
Linearity	± 4 LSB for all TPMC501 modules
ADC INL/DNL Error	± 2 LSB for INL and DNL
Physical Data	
Power Requirements	300mA typical @+5V 120mA typical @+3.3V
Temperature Range	Operating –40°C to +85°C
	Storage –40°C to +125°C
Humidity	5 – 95% non-condensing
Weight	TPMC501-1x : 78g TPMC501-2x : 63g
MTBF	TPMC501-1x : 552000 h TPMC501-2x : 578000 h

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	I/O	256	16	BIG	Local Register
1	3 (0x1C)	MEM	2K	8	BIG	Calibration Data
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Table 3-1 : PCI9030 Local Space Configuration

3.2 Local Register Address Space

PCI Base Address: **PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).**

The TPMC501 is controlled by a set of 8 registers, located in the local register address space. All registers are cleared to '0' on power up or PCI reset.

Registers CONTREG, DATAREG, STATREG, CONVERT are used for conventional mode (non sequencer mode).

Registers SEQCONT, SEQSTAT, SEQTIMER are used for "Sequencer Mode".

The sequencer instruction and data RAM are also located in this local register address space.

Offset to PCI Base Address	Register	Description	Size (Bit)	Access
0x00	CONTREG	ADC Control Register	16	R/W
0x02	DATAREG	ADC Data Register	16	R
0x04	STATREG	ADC Status Register	16	R
0x06	CONVERT	ADC Convert Start Register	16	W
0x08	INTSTAT	ADC Interrupt Status Register	16	R/W
0x0A	SEQCONT	Sequencer Control Register	16	R/W
0x0C	SEQSTAT	Sequencer Status Register	16	R/W
0x0E	SEQTIMER	Sequencer Timer Register	16	R/W
0x10	-	Reserved	-	-
...	...	...	...	
0x7F	-	Reserved	-	-
0x80-BE	SIRAM0-31	Sequencer Instruction RAM	16	R/W
0xC0-FE	SDRAM0-31	Sequencer Data RAM	16	R

Table 3-2 : Local Register Address Space

3.2.1 ADC Control Register CONTREG (Offset 0x00)

The ADC Control Register CONTREG is used to select the input channel, gain and mode for the next data conversion.

If “Sequencer Mode” is selected (SEQCONT register bit 0 set to ‘1’) write access to the ADC Control Register CONTREG is ignored.

Bit	Symbol	Description	Access	Reset Value
15:11		Write: Don’t care Read: Always ‘0’		0
10	INTENA	Interrupt Request Enable 0 = Disabled 1 = Enabled (PCI INTA line) If “Automatic Settling Time Mode” is OFF, an interrupt request is generated a) when the settling time is done, and b) when the conversion is done and data is valid in the DATAREG register. If “Automatic Settling Time Mode” is ON, an interrupt is generated when the conversion is done and data is valid in the DATAREG register.	R/W	0
9	PIPL	Pipeline Mode Control 0 = OFF Data conversion (n) is shifted into the DATAREG register after the conversion (n) is done. 1 = ON Data conversion (n-1) is shifted into the DATATREG register during the conversion (n).	R/W	0
8	Automatic	Automatic Settling Time Mode Control 0 = OFF (Normal Mode) The conversion setup is configured by the write to the CONTREG register with this bit cleared. The SETTL_BUSY bit in the STATREG register must be read as '0' before a conversion is started. A conversion is started by a write to the CONVERT register. After a conversion has been started, the next conversion may be setup by writing again to the CONTREG register. Reading the ADC_BUSY bit in the STATREG register as '0' indicates valid conversion data in the DATAREG register. 1 = ON (Automatic Mode) The data conversion is initiated by a write to the CONTREG register where this bit is set. The data conversion is automatically started when the settling time is done. Reading the ADC_BUSY bit in the STATREG register as '0' indicates valid conversion data in the DATAREG register.	R/W	0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>7:6</td><td>G[1:0]</td><td>Gain Selection (Analog Input Amplifier)

<table>
<tr><th>G1</th><th>G0</th><th>Gain Factor</th><th>Input Voltage Range</th></tr>
<tr><td colspan="4">TPMC501 -10 / -20</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>±10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>±5V</td></tr>
<tr><td>1</td><td>0</td><td>5</td><td>±2V</td></tr>
<tr><td>1</td><td>1</td><td>10</td><td>±1V</td></tr>
<tr><td colspan="4">TPMC501 -11 / -21</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>±10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>±5V</td></tr>
<tr><td>1</td><td>0</td><td>4</td><td>±2.50V</td></tr>
<tr><td>1</td><td>1</td><td>8</td><td>±1.25V</td></tr>
<tr><td colspan="4">TPMC501 -12 / -22</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0 to 10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>0 to 5V</td></tr>
<tr><td>1</td><td>0</td><td>5</td><td>0 to 2V</td></tr>
<tr><td>1</td><td>1</td><td>10</td><td>0 to 1V</td></tr>
<tr><td colspan="4">TPMC501 -13 / -23</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0 to 10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>0 to 5V</td></tr>
<tr><td>1</td><td>0</td><td>4</td><td>0 to 2.50V</td></tr>
<tr><td>1</td><td>1</td><td>8</td><td>0 to 1.25V</td></tr>
</table>
</td><td>R/W</td><td>00</td></tr>
<tr><td>5</td><td>SE/DIFF</td><td>Single/Differential Mode Control
0 = Single-ended mode
32 single ended channels are available
1 = Differential mode
16 differential channels 1 to 16 are available, channels 17 to 32 are used as - input for channels 1 to 16.
Mixed mode possible</td><td>R/W</td><td>0</td></tr>
<tr><td>4:0</td><td>CS[4:0]</td><td>Channel Select (Analog Input Channel)

<table>
<tr><th>CS[4:0]</th><th>Single-ended Channel
SE/DIFF = 0</th><th>Differential Channel
SE/DIFF = 1</th></tr>
<tr><td>00000</td><td>CH1</td><td>CH1</td></tr>
<tr><td>...</td><td>...</td><td>...</td></tr>
<tr><td>01111</td><td>CH16</td><td>CH16</td></tr>
<tr><td>...</td><td>...</td><td>N/A</td></tr>
<tr><td>11111</td><td>CH32</td><td>N/A</td></tr>
</table>
</td><td>R/W</td><td>00000</td></tr>
</table>

Table 3-3 : ADC Control Register CONTREG

3.2.2 ADC Data Register DATAREG (Offset 0x02)

Bit	Symbol	Description	Access	Reset Value
15:0	DATA	Converted Digital Data Value	R	0

Table 3-4 : 16 bit ADC Data Register DATAREG

The 16 bit data value allows direct data processing as 16 bit binary two's complement integer values.

The content of the ADC Data Register DATAREG is not valid as long as the ADC_BUSY bit in the ADC Status Register STATREG is set.

Analog Input Voltage	Digital Value TPMC501 Option -10 / -20, -11 / -21 Binary two's complement	Digital Value TPMC501 Option -12 / -22, -13 / -23 Straight binary
+ Full Scale – 1LSB	0x7FFF	0xFFFF
Midscale	0x0000	0x8000
Midscale – 1LSB	0xFFFF	0x7FFF
– Full Scale	0x8000	0x0000

Table 3-5 : ADC Data Coding

3.2.3 ADC Status Register STATREG (Offset 0x04)

Bit	Symbol	Description	Access	Reset Value
15:2		Always read as '0'	R	0
1	SETTL BUSY	SETTL_BUSY Indicates that the required settling time after a write to the CONTREG register is not yet done. If "Automatic Settling Time Mode" is OFF, this bit is set by writing to the CONTREG register. The bit is cleared when the required settling time is done. This bit must be read as '0' before a conversion is started by a write to the CONVERT register. If "Automatic Settling Time Mode" is ON, this bit should be ignored.	R	0
0	ADC BUSY	ADC_BUSY Indicates if an actual data conversion is in progress. If "Automatic Settling Time" is OFF, this bit is set by writing to the CONVERT register. If "Automatic Settling Time Mode" is ON, this bit is set by the write to the CONTREG register. This bit must be read as '0' before the conversion data is read from the DATAREG register.	R	0

Table 3-6 : ADC Status Register STATREG

3.2.4 ADC Convert Register CONVERT (Offset 0x06)

The ADC Convert Register CONVERT is a 16 bit wide write only register. The ADC Convert Register is used to start an ADC conversion when "Automatic Settling Time Mode" is OFF. The user must read the SETTL_BUSY bit in the ADC Status Register as '0' before the conversion is started. The ADC_BUSY bit in the ADC Status Register indicates if the conversion data in the ADC Data Register is valid (ADC_BUSY bit = '0').

It is allowed to set up a new channel/gain by writing to the ADC Control Register CONTREG immediately after starting an ADC conversion.

If "Sequencer Mode" is selected (SEQCONT register bit 0 is set to '1') write access to the ADC Convert Register CONVERT is ignored.

After power up the ADC is in a random state and requires two dummy conversions before operating correctly. This is based on the chip design of the ADC. All drivers from TEWS TECHNOLOGIES already include these two dummy conversions.

3.2.5 Interrupt Status Register INTSTAT (Offset 0x08)

Bit	Symbol	Description	Access	Reset Value
15:3		Always read as '0'	R	0
2	SEQ INT	Sequencer Interrupt Pending Flag (bit is controlled by the sequencer logic) If sequencer interrupts are enabled (SEQCONT register bit 1 set to '1') and a sequencer interrupt is pending (any of the SEQSTAT register bits [3:1] is '1') the sequencer interrupt pending flag is read as '1'. The interrupt is cleared by writing '1' to the corresponding status bits in the SEQSTAT register.	R	0
1	SETTL READY	SETTL_READY Interrupt Flag (bit is controlled by the settling time controller) If interrupts are enabled (CONTREG register bit 10 is set to '1') and "Automatic Settling Time Mode" is OFF (CONTREG register bit 8 is set to '0') this interrupt is generated, when the settling time is done. The interrupt is cleared by writing '1' to this bit.	R/C	0
0	ADC READY	ADC_READY Interrupt Flag (bit is controlled by the ADC controller) If interrupts are enabled (CONTREG register bit 10 is set to '1') this interrupt is generated, when a data conversion is done. The interrupt is cleared by writing '1' to this bit.	R/C	0

Table 3-7 : Interrupt Status Register INTSTAT

3.2.6 Sequencer Control Register SEQCONT (Offset 0x0A)

Bit	Symbol	Description	Access	Reset Value
15:2		Always read as '0'.	R/W	0
1	SEQ INT ENA	Sequencer Interrupts Enable Control 0 = Sequencer Interrupts disabled 1 = Sequencer Interrupts enabled (PCI INTA) An interrupt request will be generated if any bit is set in the SEQSTAT register (sequencer data valid or sequencer error).	R/W	0
0	SEQ ON	Sequencer Start / Stop Control 0 = Stops the sequencer after the last instruction 1 = Starts the sequencer immediately	R/W	0

Table 3-8 : Sequencer Control Register SEQCONT

3.2.7 Sequencer Status Register SEQSTAT (Offset 0x0C)

Bit	Symbol	Description	Access	Reset Value
15:4		Always read as '0'.	R	0
3	I-RAM ERROR	Instruction RAM Error Flag Set by the sequencer if the sequencer has been started and there is no correct instruction in the Instruction RAM. To clear this flag the user must write '1' to this bit.	R/C	0
2	TIMER ERROR	Time Error Flag Set by the sequencer if the sequencer timer expires but the actual sequence is still in progress. To clear the Timer Error Flag the user must write '1' to this bit. If the Sequencer Timer Register is 0 (Sequencer Continuous Mode) the Timer Error Flag always read as '0'.	R/C	0
1	DATA OF ERROR	Data Overflow Error Flag Set by the sequencer if the last sequencer instruction is done and the Data Available Flag of the previous sequence has not yet been cleared by the user. To clear the error flag the user must write '1' to this bit. If the Sequencer Timer Register is '0' (Sequencer Continuous Mode) the Data Overflow Error Flag always read as '0'.	R/C	0
0	DATA AV	Data Available Flag Set if a sequence is done and new ADC data is available in the ADC Data RAM. After reading the ADC Data RAM the user must clear the data Available Flag by writing '1' to this bit.	R/C	0

Table 3-9 : Sequencer Status Register SEQSTAT

As long as any of the bits [3:1] (error flags) of the Sequencer Status Register SEQSTAT is read as '1', the sequencer will be stopped after the last instruction. The user must clear the status bit and start the sequencer again.

3.2.8 Sequencer Timer Register SEQTIMER (Offset 0x0E)

The Sequencer Timer Register SEQTIMER is a 16 bit wide read/write register.

The Sequence Timer is programmable from 100µs to 6.5535s in 100µs steps.

Whenever the timer reaches the programmed value the sequencer starts a new sequence with the first instruction found in the instruction RAM.

The sequencer timer value must be chosen so that the set up sequence completes before the sequencer timer expires. If the sequence timer expires while a sequence is still in progress a timer error will be asserted.

$$Value \geq \frac{12\mu s + 14.5\mu s \cdot Number\_of\_selected\_Channels}{100\mu s} + 1$$

Figure 3-1: Sequencer Timer Value

If the Sequencer Timer Register is set to '0' the "Sequencer Continuous Mode" is selected and the sequencer will start again with the first instruction of the sequence immediately after the last instruction of the previous sequence has been completed.

3.2.9 Sequencer Instruction RAM SIRAM0-31 (Offset 0x80 to 0xBE)

The Sequencer Instruction RAM is a 32 x 16 bit wide RAM.

Each ADC channel has its own sequencer instruction word.

Offset to PCI Base Address	Channel (Instruction)	Size (Bit)
0x80	CH1 SEQ Instruction	16
0x82	CH2 SEQ Instruction	16
...	...	...
0xBC	CH31 SEQ Instruction	16
0xBE	CH32 SEQ Instruction	16

Table 3-10: Sequencer Instruction RAM SIRAM0-31

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>15:4</td><td></td><td>Write: Don’t care / Read: Always ‘0’</td><td>R/W</td><td>0</td></tr>
<tr><td>3</td><td>Enable</td><td>Enable the ADC Channel for the Sequencer
0 = Sequencer will pass over the ADC channel
1 = Sequencer converts the ADC channel and updates the ADC data in the Sequencer Data RAM at the end of the sequence
Example: If only channel 1, channel 2 and channel 8 are enabled, only the three ADC RAM locations for channel 1, channel 2 and channel 8 are updated at the end of the sequence. The user must only read these three ADC RAM locations then.</td><td>R/W</td><td>0</td></tr>
<tr><td>2:1</td><td>G[1:0]</td><td>Gain Selection (Analog Input Amplifier)
<table>
<tr><th>G1</th><th>G0</th><th>Gain Factor</th><th>Input Voltage Range</th></tr>
<tr><td colspan="4">TPMC501 -10 / -20</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>±10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>±5V</td></tr>
<tr><td>1</td><td>0</td><td>5</td><td>±2V</td></tr>
<tr><td>1</td><td>1</td><td>10</td><td>±1V</td></tr>
<tr><td colspan="4">TPMC501 -11 / -21</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>±10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>±5V</td></tr>
<tr><td>1</td><td>0</td><td>4</td><td>±2.50V</td></tr>
<tr><td>1</td><td>1</td><td>8</td><td>±1.25V</td></tr>
<tr><td colspan="4">TPMC501 -12 / -22</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0 to 10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>0 to 5V</td></tr>
<tr><td>1</td><td>0</td><td>5</td><td>0 to 2V</td></tr>
<tr><td>1</td><td>1</td><td>10</td><td>0 to 1V</td></tr>
<tr><td colspan="4">TPMC501 -13 / -23</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0 to 10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>0 to 5V</td></tr>
<tr><td>1</td><td>0</td><td>4</td><td>0 to 2.50V</td></tr>
<tr><td>1</td><td>1</td><td>8</td><td>0 to 1.25V</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
<tr><td>0</td><td>SE/DIFF</td><td>Single/Differential Mode Control
0 = Single-ended mode
32 single ended channels are available
1 = Differential mode
16 differential channels 1 to 16 are available, channels 17 to 32 are used as - input for channels 1 to 16.
Mixed mode is possible. E.g. channel 1 to channel 8 (with channels 17 to channel 24) selected as differential inputs, channel 9 to channel 16 and channel 25 to channel 32 as single-ended input channels.</td><td>R/W</td><td>0</td></tr>
</table>

Table 3-11: Sequencer Instruction Word

3.2.10 Sequencer Data RAM SDRAM0-31 (Offset 0xC0 to 0xFE)

The Sequencer Data RAM is a 32 x 16 bit wide RAM storing the converted data values.

Each ADC channel has its own ADC data location.

Offset to PCI Base Address	Channel (Converted Data)	Size (Bit)
0xC0	CH1 SEQ Data	16
0xC2	CH2 SEQ Data	16
...	...	...
0xFC	CH31 SEQ Data	16
0xFE	CH32 SEQ Data	16

Table 3-12: Sequencer Data RAM SDRAM0-31

3.3 Calibration Data ROM Space

PCI Base Address: **PCI9030 PCI Base Address 3 (Offset 0x1C in PCI Configuration Space).**

The calibration data values are determined at factory and stored in this ROM space.

The calibration data values should be used for software correction with the formulas stated below.

There is one Offset Error value and one Gain Error value for each gain.

The Offset and Gain Error values for each gain are the same for all channels 1-32.

Offset to PCI Base Address	Description			Size (Bit)
0x00	$Offset_{ERROR}$	Gain 1	High Byte	8
0x01	$Offset_{ERROR}$	Gain 1	Low Byte	8
0x02	$Gain_{ERROR}$	Gain 1	High Byte	8
0x03	$Gain_{ERROR}$	Gain 1	Low Byte	8
0x04	$Offset_{ERROR}$	Gain 2	High Byte	8
0x05	$Offset_{ERROR}$	Gain 2	Low Byte	8
0x06	$Gain_{ERROR}$	Gain 2	High Byte	8
0x07	$Gain_{ERROR}$	Gain 2	Low Byte	8
0x08	$Offset_{ERROR}$	Gain 4/5	High Byte	8
0x09	$Offset_{ERROR}$	Gain 4/5	Low Byte	8
0x0A	$Gain_{ERROR}$	Gain 4/5	High Byte	8
0x0B	$Gain_{ERROR}$	Gain 4/5	Low Byte	8
0x0C	$Offset_{ERROR}$	Gain 8/10	High Byte	8
0x0D	$Offset_{ERROR}$	Gain 8/10	Low Byte	8
0x0E	$Gain_{ERROR}$	Gain 8/10	High Byte	8
0x0F	$Gain_{ERROR}$	Gain 8/10	Low Byte	8
0x10	Reserved			
...	...			
0x7FF	Reserved			

Table 3-13: Calibration Data Values

3.3.1 Data Correction

There are two errors that affect the DC accuracy of the ADC.

ADC Offset Error:

The Offset Error is the data value when converting with the input connected to its own ground in single-ended mode, or with shorted inputs in differential mode. This error is corrected by subtracting the known error from the reading.

ADC Gain Error:

The Gain Error is the difference between the ideal gain and the actual gain of the programmable gain amplifier and the ADC. This error is corrected by multiplying the reading with a correction factor.

3.3.2 ADC Data Correction Formula

The basic formula for correcting any ADC reading for the TPMC501 -10 / -20, -11 / -21 (bipolar input voltage range) is:

$$Value = \mathrm{Re}\,ading \cdot \left(1 - \frac{Gain_{error}}{131072}\right) - \frac{Offset_{error}}{4}$$

Figure 3-2: ADC Correction Formula (Bipolar Input Range)

The basic formula for correcting any ADC reading for the TPMC501 -12 / -22, -13 / -23 (unipolar input voltage range) is:

$$Value = \mathrm{Re}\,ading \cdot \left(1 - \frac{Gain_{error}}{262144}\right) - \frac{Offset_{error}}{4}$$

Figure 3-3: ADC Correction Formula (unipolar Input Range)

Value is the corrected result.

Reading is the data read from the ADC Data Register.

$GAIN_{ERROR}$ and $OFFSET_{ERROR}$ are the correction factors from the correction ROM space, stored for each of the possible gains.

The correction values are stored as two's complement 16 bit wide values in the range –32768 to 32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic must be used to avoid rounding errors while computing above formula.

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	9050 10B5
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	118000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFF01
0x1C	PCI Base Address 3 for Local Address Space 1				Y	FFFFF800
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	01F5 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 48 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 4C 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 4-1 : PCI9030 Header

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FF01
0x04	Local Address Space 1 Range	0x0FFF_F800
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Expansion ROM Range	0x0000_0000
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_0801
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_0000
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000
0x28	Local Address Space 0 Bus Region Descriptor	0x8150_2840
0x2C	Local Address Space 1 Bus Region Descriptor	0xE933_79C0
0x30	Local Address Space 2 Bus Region Descriptor	0x0000_0000
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0041
0x40	Chip Select 1 Base Address	0x0000_00A1
0x44	Chip Select 2 Base Address	0x0000_00E1
0x48	Chip Select 3 Base Address	0x0000_0C01
0x4C	Interrupt Control/Status	0x0049
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x0078_0000
0x54	General Purpose I/O Control	0x0400_0B60
0x70	Hidden1 Register for Power Management Data Select	0x0000_0000
0x74	Hidden 2 Register for Power Management Data Scale	0x0000_0000

Table 4-2 : PCI9030 Local Configuration Registers

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9050	0x10B5	0x0280	0x0000	0x1180	0x0000	0x01F5	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFF01	0x0FFF	0xF800
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0801	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x8150	0x2840	0xE933	0x79C0	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0041	0x0000	0x00A1	0x0000	0x00E1
0x70	0x0000	0x0C01	0x0030	0x0049	0x0078	0x0000	0x0000	0x0240
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM TPMC501-xx

4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

5 Operation Modes

The TPMC501 supports four conventional operating modes (non sequencer modes) which are selected with bit 8 (Automatic Mode OFF / ON) and bit 9 (Pipeline Mode OFF / ON) of the ADC Control Register CONTREG.

A sequencer operating mode is also provided using the sequencer registers.

5.1 Conventional Modes

- Normal Mode without Data Pipeline
- Normal Mode with Data Pipeline
- Automatic Mode without Data Pipeline
- Automatic Mode with Data Pipeline

	CONTREG Bit 8 = 0 Normal Mode	**CONTREG Bit 8 = 1 Automatic Mode**
CONTREG Bit 9 = 0 Data Pipeline OFF	A write access to the CONVERT register starts conversion N and shifts the result of conversion N into the DATAREG register	After the settling time has expired conversion N is started and the result of conversion N is shifted into the DATAREG register
CONTREG Bit 9 = 1 Data Pipeline ON	A write access to the CONVERT register starts conversion N and shifts the result of conversion N-1 into the DATAREG register	After the settling time has expired conversion N is started and the result of conversion N-1 is shifted into the DATAREG register

Table 5-1 : Conventional Operating Modes

In "Normal Mode" the SETTL_BUSY flag in the ADC Status Register STATREG must be read as '0' before a conversion is started by writing to the ADC Convert Register CONVERT.

5.1.1 Normal Mode

Any write access to the CONTREG register where bit 8 is set to '0' selects the "Normal Mode" with the selected input channel, input channel mode and gain.

As long as the analog input path settling time has not expired, the SETTL_BUSY flag in the STATREG register is read as ‘1‘. After the settling time has expired (SETTL_BUSY flag = '0') a conversion can be started by writing to the CONVERT register.

The conversion data is available in the DATAREG register, when the ADC_BUSY flag in the STATREG register is read as '0'.

It is possible, to select a next channel and / or gain by writing to the CONTREG register, immediately after the actual conversion has been started by writing to the CONVERT register. In this mode the settling time for the next channel and the conversion time of the actual channel proceed simultaneously. As long as the ADC_BUSY flag in the STATREG register is read as ‘1‘ the actual conversion is still in progress. Reading the ADC_BUSY flag as ‘0‘ indicates that the conversion result is available in the DATAREG register.

If interrupts are enabled, two interrupts will be generated: the first interrupt when the settling time is done after writing to the CONTREG register, the second interrupt when the data conversion is done after writing to the CONVERT register.

If “Normal Mode without Data Pipeline” is selected, the result of the actual conversion is shifted into the DATAREG register. In this mode it is possible that the settling time and conversion time proceed simultaneously. The total acquisition and conversion time in this mode is 22.5µs.

If “Normal Mode with Data Pipeline” is selected, during conversion N the result of conversion N-1 is shifted into the DATAREG register. In this mode it is possible that the settling time and conversion time proceed simultaneously. The total acquisition and conversion time in this mode is 14.5µs with channel / gain change.

5.1.1.1 Normal Mode without Data Pipeline

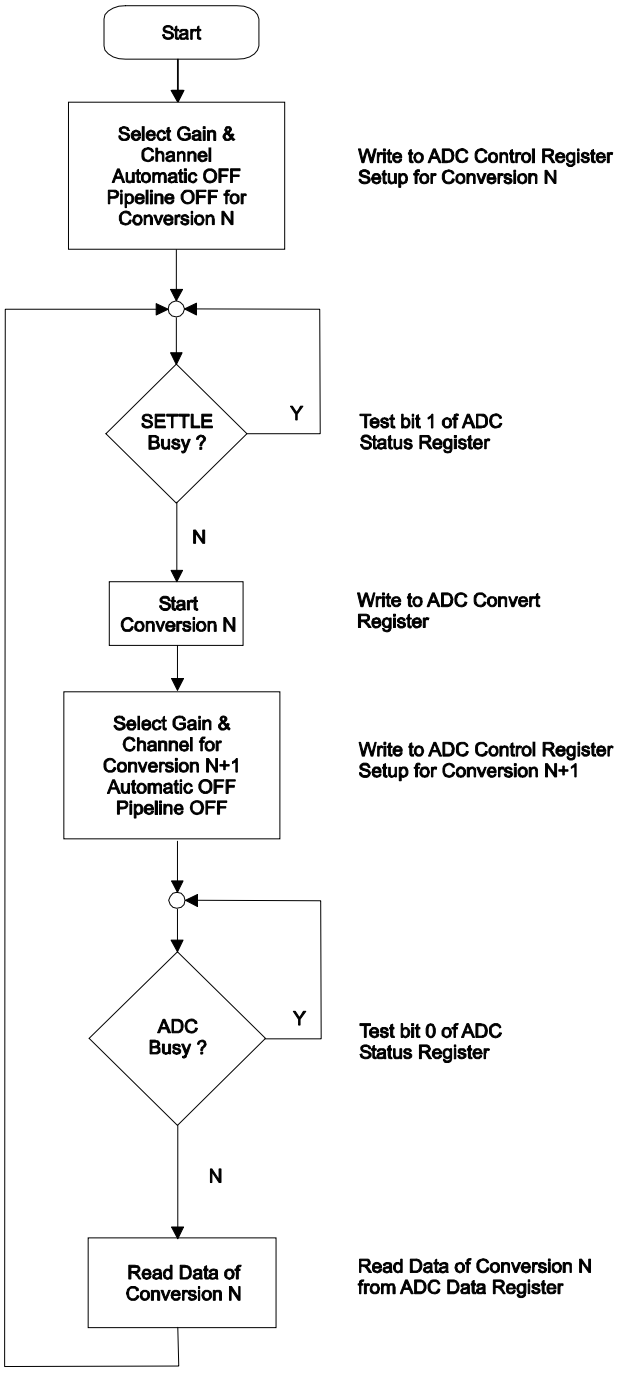

Figure 5-1 : Normal Mode without Data Pipeline Flow

For subsequent ADC conversions without changing channel or gain it is not necessary to test the SETTL_BUSY bit in the ADC Status Register STATREG.

5.1.1.2 Normal Mode with Data Pipeline

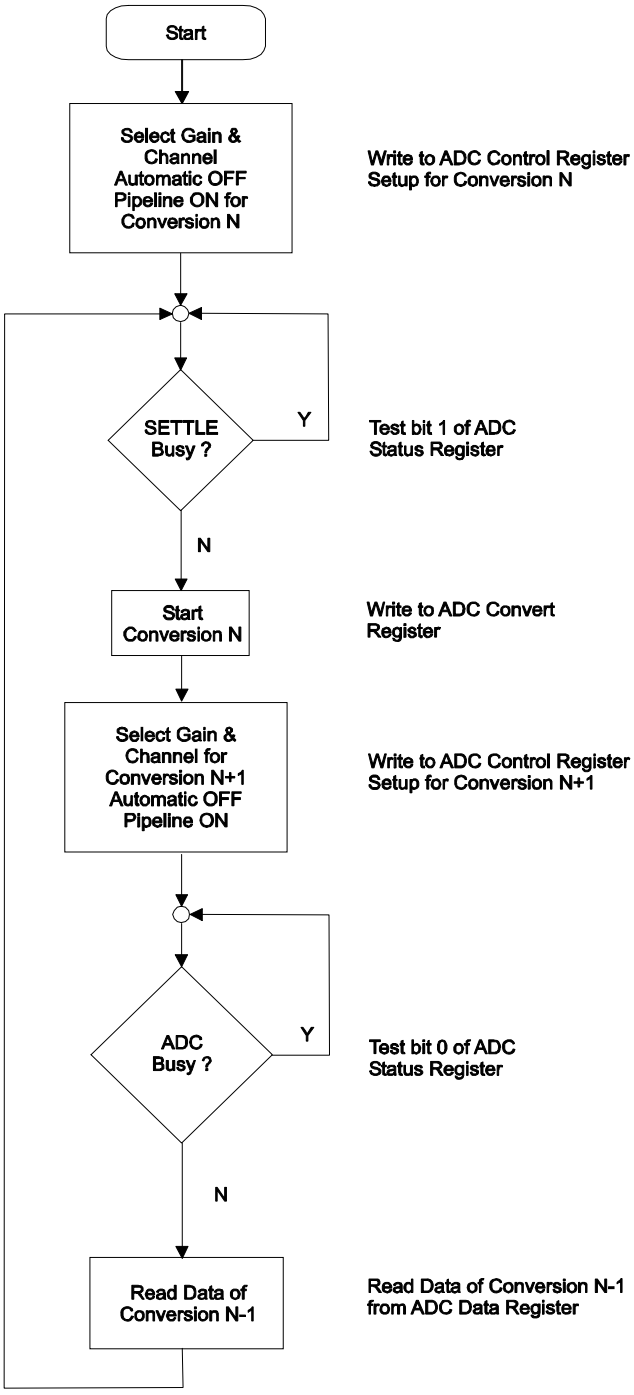

Figure 5-2 : Normal Mode with Data Pipeline Flow

For subsequent ADC conversions without changing channel or gain it is not necessary to test the SETTL_BUSY bit in the ADC Status Register STATREG.

5.1.2 Automatic Mode

Any write access to the CONTREG register where bit 8 is set to '1' selects the "Automatic Mode" with the selected input channel, input channel mode and gain.

The data conversion is started automatically by hardware when the settling time has expired.

The conversion data is available in the DATAREG register, when the ADC_BUSY flag in the STATREG register is read as '0'.

If interrupts are enabled, an interrupt is generated when the data conversion is done.

If “Automatic Mode without Data Pipeline” is selected the result of the actual conversion is shifted into the DATAREG register. The acquisition and conversion time in this mode is 32.5µs.

If “Automatic Mode with Data Pipeline” is selected, during conversion N, the result of conversion N-1 is shifted into the DATAREG register. The acquisition and conversion time in this mode is 22.5µs.

5.1.2.1 Automatic Mode without Data Pipeline

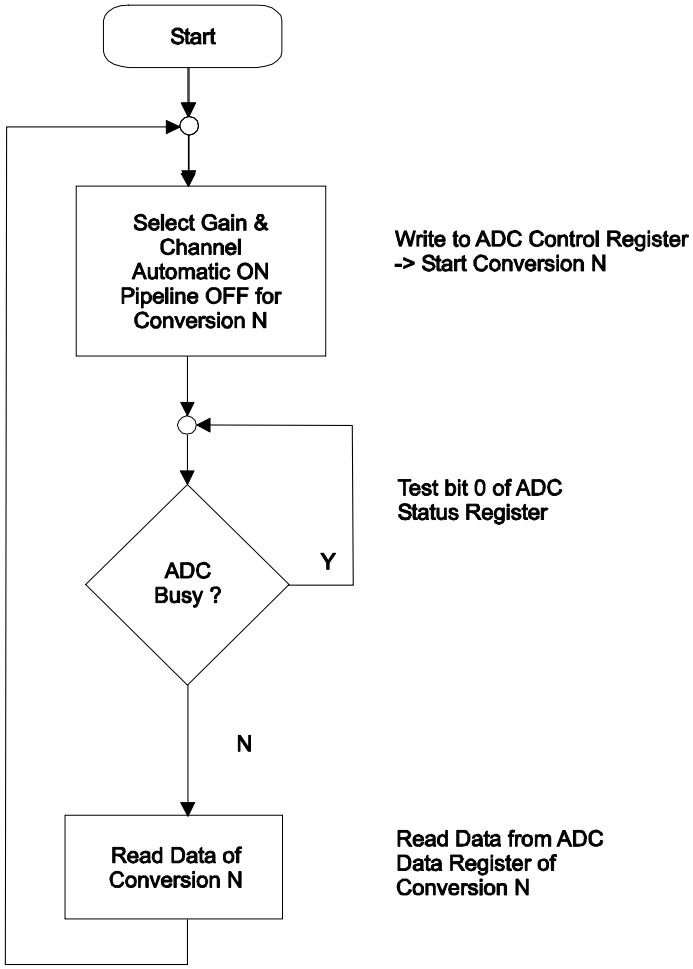

Figure 5-3 : Automatic Mode without Data Pipeline Flow

5.1.2.2 Automatic Mode with Data Pipeline

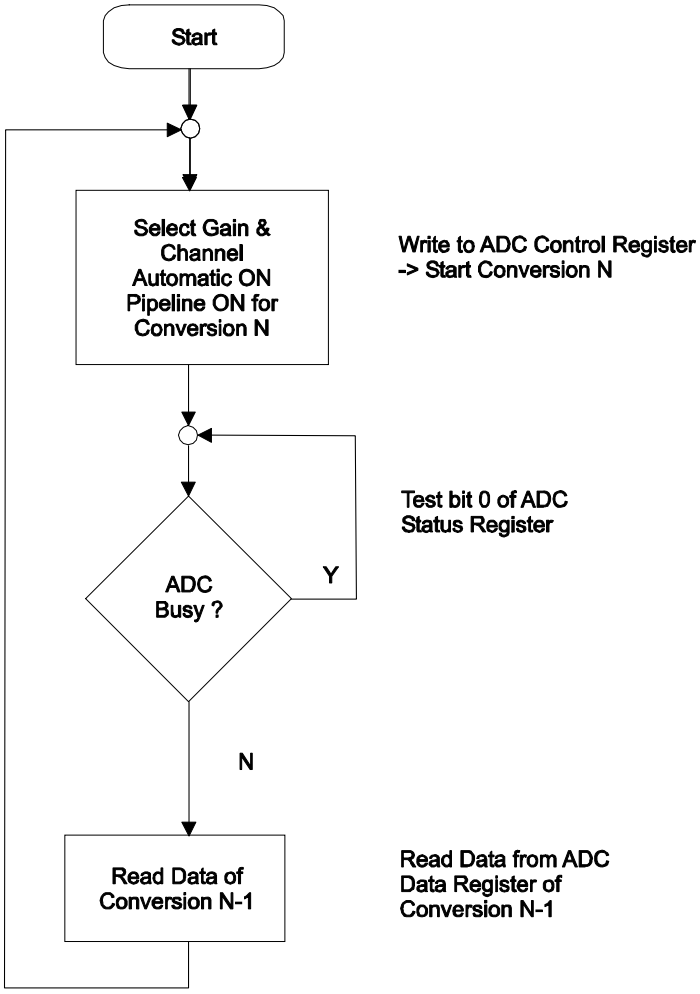

Figure 5-4 : Automatic Mode with Data Pipeline Flow

5.2 Sequencer Mode

The “Sequencer Mode” is very useful for periodic measurements. The sequencer converts all enabled ADC channels and stores the results in the Sequencer Data RAM. After a programmable time the sequencer repeats this sequence.

To use the sequencer, first each channel must be configured for the sequence using the Sequencer Instruction RAM. In the Sequencer Instruction RAM there is a sequencer instruction word for each channel. The sequencer instruction word is used to enable a channel for the sequence and to select gain and mode (single-ended or differential) for that channel.

If the sequencer is started, all enabled channels, beginning from channel 1 forward to 32, will be converted and the results are stored in the Sequencer Data RAM at the end of the sequence. When the last sequencer instruction word has been completed the data available flag located in the Sequencer Status Register SEQSTAT is set to ‘1’ and if enabled, an interrupt request will be asserted. If the data available flag is read as ‘1’ the user can read the ADC data from the Sequencer Data RAM (only the enabled channels are updated). After that, the user must clear the data available flag by writing a ‘1’ to Sequencer Status Register SEQSTAT bit 0.

The repeat frequency of the sequencer can be programmed by using the Sequencer Timer. The Sequencer Timer is programmable from 100µs to 6.5535s in 100µs steps. Whenever the timer reaches the programmed value, the sequencer starts a new sequence.

A special function is the "Sequencer Continuous Mode". It is activated if the Sequencer Timer Register is set to 0x0000. In this mode the sequencer will immediately start a new sequence when the actual sequence has been completed. When the sequencer is in “Sequencer Continuous Mode” the user can read valid data from the Sequencer Data RAM at any time. The Sequencer Data RAM locations of the enabled ADC channels are updated as soon as possible.

The update rate depends on the number of enabled channels.

$$update\_rate \leq 12\mu s + 14.5\mu s \cdot Number\_of\_enabled\_channels$$

5.2.1 Sequencer Errors

If the sequencer detects an error, it will stop after the last instruction and sets the corresponding error flag in the Sequencer Status Register SEQSTAT.

Error	Description	Sequencer Action	User Action
Data Overflow Error	Error occurs if the sequencer has new data to store but the user has not yet acknowledged that the data from the previous sequence has been read out. (Sequencer Timer Mode only)	Sequencer stops after the last instruction is done. Data Overflow Error Flag is set. If enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 1. Make sure the sequencer data is read and acknowledged within the programmed sequence time. Start sequencer again.
Timer Error	Error occurs if the programmed Sequencer Time is shorter than the sequence itself. (Sequencer Timer Mode only)	Sequencer stops after the last instruction is done. Timer Error Flag is set. If enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 2. Program a larger sequence time. Start sequencer again.
Instruction RAM Error	Error occurs if no channel is enabled for the sequence (bit 3 of Sequencer Instruction RAM word) and the sequencer is started.	Sequencer stops after the last instruction is done. Instruction RAM Error Flag is set. If it is enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 3. Correct the Sequencer Instruction RAM setting. Start sequencer again.

Table 5-2 : Sequencer Errors

If the Sequence Timer Register is set to 0x0000 (Sequencer Continuous Mode) the sequencer ignores the data overflow. The Data Overflow Error Flag is always read as '0' in this mode.

5.2.2 Sequencer Mode Flow

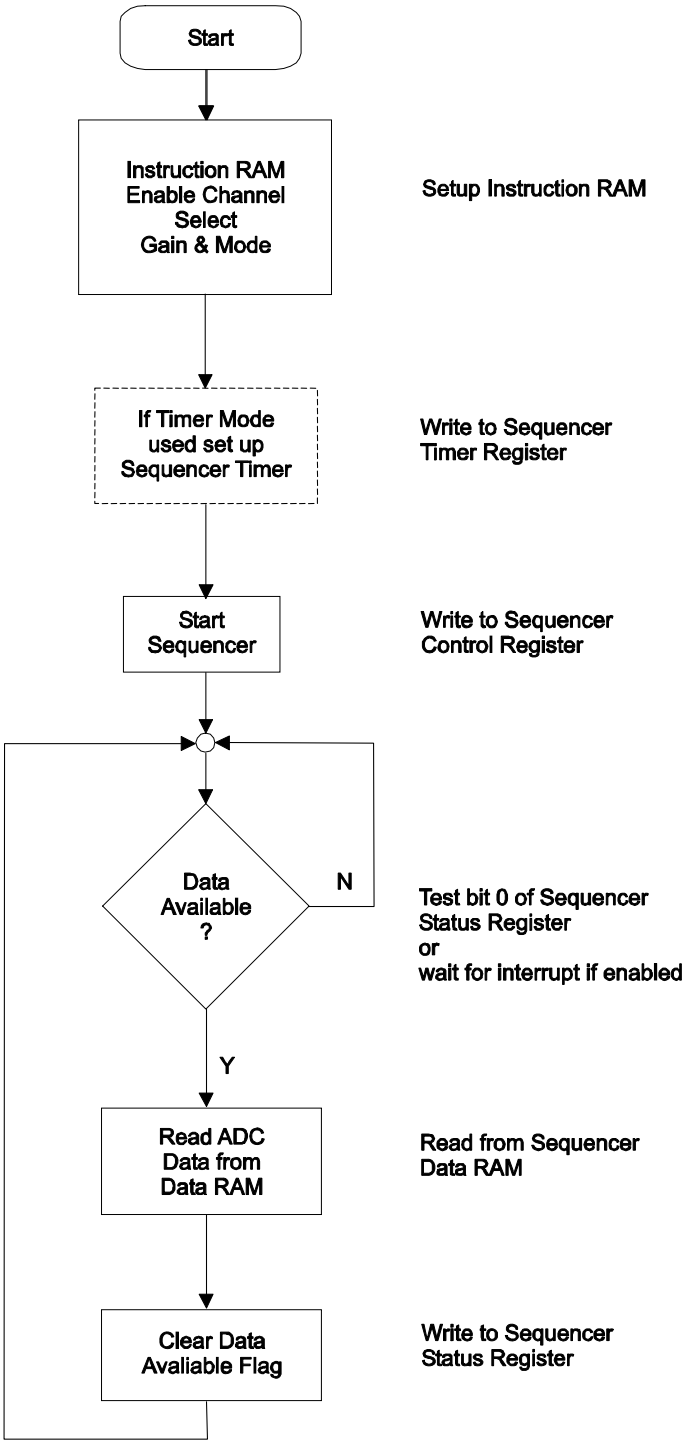

Figure 5-5 : Sequencer Mode Flow

6 Pin Assignment

6.1 Pin Assignment HD50 Connector / P14 I/O

HD50 connector (TPMC501-1x) P14 I/O (TPMC501-2x)	I/O Signal Single-Ended Mode	I/O Signal Differential Mode
01	ADC_IN_1	ADC_IN_1 +
02	ADC_IN_17	ADC_IN_1 -
03	A_GND	A_GND
04	A_GND	A_GND
05	ADC_IN_2	ADC_IN_2 +
06	ADC_IN_18	ADC_IN_2 -
07	ADC_IN_3	ADC_IN_3 +
08	ADC_IN_19	ADC_IN_3 -
09	A_GND	A_GND
10	A_GND	A_GND
11	ADC_IN_4	ADC_IN_4 +
12	ADC_IN_20	ADC_IN_4 -
13	ADC_IN_5	ADC_IN_5 +
14	ADC_IN_21	ADC_IN_5 -
15	A_GND	A_GND
16	A_GND	A_GND
17	ADC_IN_6	ADC_IN_6 +
18	ADC_IN_22	ADC_IN_6 -
19	ADC_IN_7	ADC_IN_7 +
20	ADC_IN_23	ADC_IN_7 -
21	A_GND	A_GND
22	A_GND	A_GND
23	ADC_IN_8	ADC_IN_8 +
24	ADC_IN_24	ADC_IN_8 -
25	ADC_IN_9	ADC_IN_9 +
26	ADC_IN_25	ADC_IN_9 -
27	A_GND	A_GND
28	A_GND	A_GND
29	ADC_IN_10	ADC_IN_10 +
30	ADC_IN_26	ADC_IN_10 -
31	ADC_IN_11	ADC_IN_11 +
32	ADC_IN_27	ADC_IN_11 -
33	A_GND	A_GND
34	A_GND	A_GND
35	ADC_IN_12	ADC_IN_12 +
36	ADC_IN_28	ADC_IN_12 -

HD50 connector (TPMC501-1x) P14 I/O (TPMC501-2x)	I/O Signal Single-Ended Mode	I/O Signal Differential Mode
37	ADC_IN_13	ADC_IN_13 +
38	ADC_IN_29	ADC_IN_13 -
39	A_GND	A_GND
40	A_GND	A_GND
41	ADC_IN_14	ADC_IN_14 +
42	ADC_IN_30	ADC_IN_14 -
43	ADC_IN_15	ADC_IN_15 +
44	ADC_IN_31	ADC_IN_15 -
45	A_GND	A_GND
46	A_GND	A_GND
47	ADC_IN_16	ADC_IN_16 +
48	ADC_IN_32	ADC_IN_16 -
49	Not used	Not used
50	Not used	Not used
51 (P14 I/O only)	Not used	Not used
...	...	...
64 (P14 I/O only)	Not used	Not used

Table 6-1 : I/O Pin Assignment

The TPMC501-1x options provide front panel I/O on a HD50 female connector (SCSI-2 type).

The TPMC501-2x options provide back I/O on the P14 64-pin PMC connector.

7 Programming Note

After power up the on board ADC device is in a random state and requires two dummy conversions before operating correctly. This is based on the chip design of the ADC device.

Software should ignore the data of the first two ADC conversions after power-up.

The software drivers from TEWS TECHNOLOGIES already include these two dummy conversions.

8 Installation Note

Make sure that all unused analog input pins are tied to the AGND signal level (or any other valid signal level within the analog input voltage range). This is required even if the unused channels are turned off by software.

If unused analog inputs are left floating, they could badly degrade the performance of the active channels.