The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC551

8/4 Channels of Isolated 16-bit D/A

Version 1.1

User Manual

Issue 1.1.0

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TPMC551-10

8 channels of isolated 16-bit D/A, front panel I/O

TPMC551-11

4 channels of isolated 16-bit D/A, front panel I/O

TPMC551-20

8 channels of isolated 16-bit D/A, P14 I/O

TPMC551-21

4 channels of isolated 16-bit D/A, P14 I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	June 1999
1.1	Additions to Technical Specifications	March 2000
1.2	General Corrections	June 2000
1.3	General Revision	January 2003
1.4	New address TEWS LLC	September 2006
1.5	Corrected Board Options in Technical Specification Table	September 2006
1.1.0	- New Board Revision - New versioning scheme for User Manuals - Corrected Description of VR2 and VR1 in Table “DAC Status Register”	July 2009

Table of Contents

List of Figures

List of Tables

1 Product Description

The TPMC551 is a standard single-width 32-bit PMC module providing optically isolated 16-bit analog outputs.

The number of D/A channels and the I/O connector depends on the module version:

TPMC551-10: 8 channels of isolated 16-bit D/A with front panel I/O

TPMC551-11: 4 channels of isolated 16-bit D/A with front panel I/O

TPMC551-20: 8 channels of isolated 16-bit D/A, P14 I/O

TPMC551-21: 4 channels of isolated 16-bit D/A, P14 I/O

Settling time to 0.003% is 10µs typical. Immediate and simultaneous loading are supported.

A sequencer allows periodical updates of enabled channels and the sequence timer range extends from 100µs to 6.5s.

The TPMC551 offers two output voltage ranges, ±10 V and 0-10V, which are selectable by solder pads. An on board DC/DC converter powers the isolated DAC and the output buffers.

Each TPMC551 is delivered factory calibrated. The calibration information is stored in the Calibration-PROM unique to each PMC module.

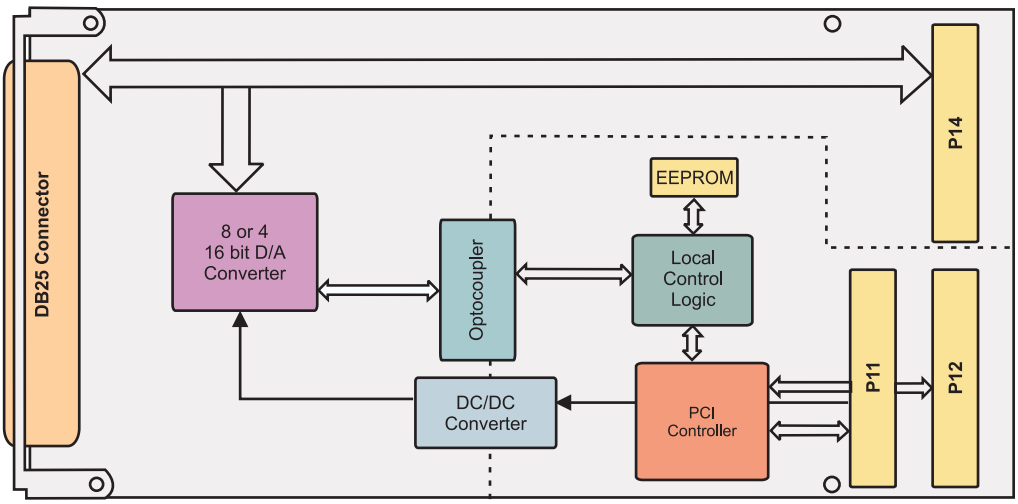

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	PCI9030 (PLX Technology)
D/A Converter	AD7840CR
Digital-to-Analog Conversion	
Resolution	16-bit
Output Voltage Range	0…+10V or ±10V, selectable for a group of four channels
Output Settling Time	10V steps: 7µs typical, 10µs maximum
Output Load per Channel	Max. 4mA, 1000pF
I/O Interface	
Number of Channels	TPMC551-x0: 8 channels TPMC551-x1: 4 channels
I/O Connector	TPMC551-1x: DB25 female connector, front panel (Harting part#: 0966 352 6616) TPMC551-2x: PMC P14 I/O 64 pin Mezzanine Connector
Physical Data	
Power Requirements	TPMC551-x0: 120mA typical @ +3.3V DC 750mA typical @ +5V DC TPMC551-x1: 120mA typical @ +3.3V DC 450mA typical @ +5V DC
Temperature Range	Operating: -40°C to +85°C Storage: -40°C to +125°C
MTBF	TPMC551-10: 371000h TPMC551-11: 512000h TPMC551-20: 353000h TPMC551-21: 479000h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	TPMC551-1x: 78g TPMC551-2x: 74g

Table 2-1 : Technical Specifications

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by addressing the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	I/O	32	16	BIG	Register & Sequencer RAM Space
1	3 (0x1C)	MEM	64	8	BIG	Calibration Data Space

Table 3-1 : PCI9030 Local Space Configuration

3.2 Register & Sequencer RAM Space

The Register & Sequencer RAM Space includes the DAC and Sequencer Registers as well as the Sequencer Data RAM.

PCI Base Address: **PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).**

Offset to PCI Base Address 2	Symbol	Register Name	Size (Bit)	Access
0x00	DAC_CTRL	DAC Control Register	16	R/W
0x02	DAC_DATA	DAC Data Register	16	R/W
0x04	DAC_STAT	DAC Status Register	16	R
0x06	DAC_CONV	DAC Convert Register	16	R/W
0x08	SEQ_CTRL	Sequencer Control Register	16	R/W
0x0A	SEQ_STAT	Sequencer Status Register	16	R/C
0x0C	SEQ_TIME	Sequencer Timer Register	16	R/W
0x0E	-	Reserved	-	-
0x10	SEQ_DATA_CH1	Sequencer Data Channel 1 Register	16	W
0x12	SEQ_DATA_CH2	Sequencer Data Channel 2 Register	16	W
0x14	SEQ_DATA_CH3	Sequencer Data Channel 3 Register	16	W
0x16	SEQ_DATA_CH4	Sequencer Data Channel 4 Register	16	W
0x18	SEQ_DATA_CH5	Sequencer Data Channel 5 Register	16	W
0x1A	SEQ_DATA_CH6	Sequencer Data Channel 6 Register	16	W
0x1C	SEQ_DATA_CH7	Sequencer Data Channel 7 Register	16	W
0x1E	SEQ_DATA_CH8	Sequencer Data Channel 8 Register	16	W

Table 3-2 : Register & Sequencer RAM Space Address Map

3.2.1 DAC Control Register (Offset 0x00)

The DAC Control Register (DAC_CTRL) is used to reset the DAC outputs. The output voltage is 0V in both output voltage ranges.

Bit	Symbol	Description	Access	Reset Value
15:1	-	Not used, always read as '0'		
0	DRST	DAC Reset Bit (used to hold all DAC outputs in reset state): 0 = DAC outputs of all channels are in operating mode 1 = DAC outputs of all channels are forced to reset state (0V output voltage)	R/W	0

Table 3-3 : DAC Control Register

The analog DAC outputs of all channels are also held in reset state for the time of a PCI reset or local reset.

3.2.2 DAC Data Register (Offset 0x02)

The DAC Data Register (DAC_DATA) stores the 16-bit data value for the next D/A conversion.

Bit	Symbol	Description	Access	Reset Value
15:0	-	16-bit Data Value for next D/A Conversion	R/W	0x0000

Table 3-4 : DAC Data Register

3.2.3 DAC Status Register (Offset 0x04)

The DAC Status Register (DAC_STAT) indicates DAC status conditions.

Bit	Symbol	Description	Access	Reset Value
15:4	-	Not used, always read as ‘0’	R	
3	NRCH	This Bit indicates the number of available D/A channels: 0 = 4 D/A channels are available (TPMC551-11, TPMC551-21) 1 = 8 D/A channels are available (TPMC551-10, TPMC551-20)	R	X
2	VR2	Output Voltage Range for D/A channels 5 to 8: 0 = D/A channels 5 to 8 are set to 0…10V output voltage range 1 = D/A channels 5 to 8 are set to ±10V output voltage range This bit is only valid for variants TPMC551-10 and TPMC551-20	R	X
1	VR1	Output Voltage Range for D/A channels 1 to 4: 0 = D/A channels 1 to 4 are set to 0…10V output voltage range 1 = D/A channels 1 to 4 are set to ±10V output voltage range	R	X
0	DBSY	DAC Busy (Bit indicates an active D/A conversion) 0 = No D/A conversion in progress 1 = D/A conversion in progress The DBSY bit must be read as '0' before a conversion is started by writing to the DAC_CONV register.	R	0

Table 3-5 : DAC Status Register

3.2.4 DAC Convert Register (Offset 0x06)

The DAC Convert register (DAC_CONV) is used to start a D/A conversion. The D/A channel and the conversion mode are set up in the same write access that starts the D/A conversion. The conversion uses the data value stored in the DAC data register. Please refer to chapter “Functional Description” for detailed information about the available modes of operation.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>15:5</td><td>-</td><td>Not used, always read as ‘0’</td><td>-</td><td>-</td></tr>
<tr><td>4</td><td>DLDC</td><td>DAC Load Command:

0 = Transparent or Latched Load Mode
(actual DAC Load Mode depends on DLDM bit)
1 = Simultaneous Load Command
(all D/A channel outputs are updated according to the previously loaded DAC channel registers)

For DLDC = 1 (Simultaneous Load Command) the bits 3:0 should be written as “0000”.</td><td>R/W</td><td>0</td></tr>
<tr><td>3</td><td>DLDM</td><td>DAC Load Mode:

0 = Transparent Mode
(Load selected DAC channel register and update D/A channel analog output immediately)
1 = Latched Mode
(Loads selected DAC channel register only, the D/A channel analog output is not updated)

Use the latched mode to load the desired D/A channel registers for a following simultaneous load command.</td><td>R/W</td><td>0</td></tr>
<tr><td>2
1
0</td><td>DCH2
DCH1
DCH0</td><td>DAC Channel selection for D/A conversion:
<table>
<tr><th>DCH2</th><th>DCH1</th><th>DCH0</th><th>Selected DAC Channel</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DAC Channel 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DAC Channel 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DAC Channel 3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DAC Channel 4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>DAC Channel 5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DAC Channel 6</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>DAC Channel 7</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DAC Channel 8</td></tr>
</table></td><td>R/W</td><td>000</td></tr>
</table>

Table 3-6 : DAC Convert Register

The DBSY bit in the DAC_STAT register must be read as '0' before a conversion is started by writing to the DAC_CONV register.

3.2.5 Sequencer Control Register (Offset 0x08)

The Sequencer Control register is used to setup channels and modes for the sequencer mode.

Bit	Symbol	Description	Access	Reset Value
15	CH8E	The CHxE bits are used to enable or disable DAC channel x for the next sequence: 0 = DAC channel x is disabled 1 = DAC channel x is enabled	R/W	0x00
14	CH7E			
13	CH6E			
12	CH5E			
11	CH4E			
10	CH3E			
9	CH2E			
8	CH1E			
7:4	-	Not used, always read as '0'	-	-
3	INTE	Sequencer Interrupt Enable: 0 = Interrupts disabled 1 = Interrupts enabled The only interrupt source is the SDAT status bit in the SEQ_STAT register. Interrupts are requested at the LINT1 input of the PCI 9030 Target Chip.	R/W	0
2	SLMD	Sequencer Load Mode: 0 = Transparent Mode (The analog output of each enabled DAC channel is updated as soon as possible within the sequence) 1 = Latched Mode (The analog outputs of all DAC channels are updated simultaneously at the end of the sequence)	R/W	0
1	STMD	Sequencer Runaround Mode: 0 = Continuous mode (The next sequence starts immediately after the actual sequence is done) 1 = Timer mode (The next sequence starts when the sequencer timer has expired)	R/W	0
0	SEQE	Sequencer Enable: 0 = Sequencer disabled (an actual sequence in progress will complete) 1 = Sequencer enabled (starts the sequencer mode)	R/W	0

Table 3-7 : Sequencer Control Register

3.2.6 Sequencer Status Register (Offset 0x0A)

The Sequencer Status register indicates sequencer conditions.

Bit	Symbol	Description	Access	Reset Value
15:2	-	Not used, always read as '0'	-	-
1	SUFL	Sequencer Data Underflow: 1 = Sequencer Data Underflow (Sequencer is ready for the next sequence but the user has not yet confirmed new data in sequencer data RAM) This Bit is cleared by writing a '1'.	R/C	0
0	SDAT	Sequencer Data Request/Acknowledge: 1 = Sequencer Data Request (Sequencer is requesting new data in the sequencer data RAM) During sequencer mode this status bit must be cleared by the user after the sequencer data RAM has been updated with data for the next sequence. This Bit is cleared by writing a '1'.	R/C	0

Table 3-8 : Sequencer Status Register

Bit 0 (SDAT) of the Sequencer Status Register can assert an interrupt request (PCI9030 LINT1) if interrupts are enabled in the Sequencer Control register. SDAT must be cleared for interrupt acknowledgement.

3.2.7 Sequencer Timer Register (Offset 0x0C)

The Sequencer Timer register is used to set up the time for the sequencer timer mode.

Bit	Symbol	Description	Access	Reset Value
15:0	SEQ_TIME	16-bit Sequencer Timer Value The step size is 100µs, i.e. the time can be set to a value between 0s and 6.5535s in 100µs steps.	R/W	0x0000

Table 3-9 : Sequencer Timer Register

The sequencer timer is loaded with the value in the sequencer timer register when a sequence is started. In sequencer timer mode the start of the next sequence is delayed until the sequencer timer expires. A timer value of 0 effectively puts the sequencer into continuous mode.

The time base for the sequencer timer is derived from an on board 32 MHz oscillator.

3.2.8 Sequencer Data RAM (Offset 0x10 – 0x1E)

The Sequencer Data RAM is an 8 x 16-bit write-only RAM space that stores the conversion data for all eight DAC channels in sequencer mode.

Each 16-bit word stores the conversion data for a D/A channel. The data structure and data coding is the same as for the DAC Data Register.

Offset to PCI Base Address	Function
0x10	Conversion Data for DAC channel 1
0x12	Conversion Data for DAC channel 2
0x14	Conversion Data for DAC channel 3
0x16	Conversion Data for DAC channel 4
0x18	Conversion Data for DAC channel 5
0x1A	Conversion Data for DAC channel 6
0x1C	Conversion Data for DAC channel 7
0x1E	Conversion Data for DAC channel 8

Table 3-10 : Sequencer Data RAM

3.3 Calibration Data Space

The DAC Calibration Data is mapped to the PCI9030 Local Address Space 1.

PCI Base Address: PCI9030 PCI Base Address 3 (Offset 0x1C in PCI Configuration Space).

The DAC Calibration Data Space stores the factory calibration data (offset and gain error) for each DAC channel.

See the Programming Hints chapter for data correction formulas.

The calibration data is read only.

Offset to PCI Base Address	DAC Correction Data	Value
Calibration Data for 0…+10V Output Voltage Range		
0x00	DAC Channel 1 Offset Error High Byte	Board dependent
0x01	DAC Channel 1 Offset Error Low Byte	Board dependent
0x02	DAC Channel 2 Offset Error High Byte	Board dependent
0x03	DAC Channel 2 Offset Error Low Byte	Board dependent
0x04	DAC Channel 3 Offset Error High Byte	Board dependent
0x05	DAC Channel 3 Offset Error Low Byte	Board dependent
0x06	DAC Channel 4 Offset Error High Byte	Board dependent
0x07	DAC Channel 4 Offset Error Low Byte	Board dependent
0x08	DAC Channel 5 Offset Error High Byte	Board dependent
0x09	DAC Channel 5 Offset Error Low Byte	Board dependent
0x0A	DAC Channel 6 Offset Error High Byte	Board dependent
0x0B	DAC Channel 6 Offset Error Low Byte	Board dependent
0x0C	DAC Channel 7 Offset Error High Byte	Board dependent
0x0D	DAC Channel 7 Offset Error Low Byte	Board dependent
0x0E	DAC Channel 8 Offset Error High Byte	Board dependent
0x0F	DAC Channel 8 Offset Error Low Byte	Board dependent
0x10	DAC Channel 1 Gain Error High Byte	Board dependent
0x11	DAC Channel 1 Gain Error Low Byte	Board dependent
0x12	DAC Channel 2 Gain Error High Byte	Board dependent
0x13	DAC Channel 2 Gain Error Low Byte	Board dependent
0x14	DAC Channel 3 Gain Error High Byte	Board dependent
0x15	DAC Channel 3 Gain Error Low Byte	Board dependent
0x16	DAC Channel 4 Gain Error High Byte	Board dependent
0x17	DAC Channel 4 Gain Error Low Byte	Board dependent
0x18	DAC Channel 5 Gain Error High Byte	Board dependent
0x19	DAC Channel 5 Gain Error Low Byte	Board dependent
0x1A	DAC Channel 6 Gain Error High Byte	Board dependent
0x1B	DAC Channel 6 Gain Error Low Byte	Board dependent

Offset to PCI Base Address	DAC Correction Data	Value
0x1C	DAC Channel 7 Gain Error High Byte	Board dependent
0x1D	DAC Channel 7 Gain Error Low Byte	Board dependent
0x1E	DAC Channel 8 Gain Error High Byte	Board dependent
0x1F	DAC Channel 8 Gain Error Low Byte	Board dependent
Calibration Data for +/-10V Output Voltage Range		
0x20	DAC Channel 1 Offset Error High Byte	Board dependent
0x21	DAC Channel 1 Offset Error Low Byte	Board dependent
0x22	DAC Channel 2 Offset Error High Byte	Board dependent
0x23	DAC Channel 2 Offset Error Low Byte	Board dependent
0x24	DAC Channel 3 Offset Error High Byte	Board dependent
0x25	DAC Channel 3 Offset Error Low Byte	Board dependent
0x26	DAC Channel 4 Offset Error High Byte	Board dependent
0x27	DAC Channel 4 Offset Error Low Byte	Board dependent
0x28	DAC Channel 5 Offset Error High Byte	Board dependent
0x29	DAC Channel 5 Offset Error Low Byte	Board dependent
0x2A	DAC Channel 6 Offset Error High Byte	Board dependent
0x2B	DAC Channel 6 Offset Error Low Byte	Board dependent
0x2C	DAC Channel 7 Offset Error High Byte	Board dependent
0x2D	DAC Channel 7 Offset Error Low Byte	Board dependent
0x2E	DAC Channel 8 Offset Error High Byte	Board dependent
0x2F	DAC Channel 8 Offset Error Low Byte	Board dependent
0x30	DAC Channel 1 Gain Error High Byte	Board dependent
0x31	DAC Channel 1 Gain Error Low Byte	Board dependent
0x32	DAC Channel 2 Gain Error High Byte	Board dependent
0x33	DAC Channel 2 Gain Error Low Byte	Board dependent
0x34	DAC Channel 3 Gain Error High Byte	Board dependent
0x35	DAC Channel 3 Gain Error Low Byte	Board dependent
0x36	DAC Channel 4 Gain Error High Byte	Board dependent
0x37	DAC Channel 4 Gain Error Low Byte	Board dependent
0x38	DAC Channel 5 Gain Error High Byte	Board dependent
0x39	DAC Channel 5 Gain Error Low Byte	Board dependent
0x3A	DAC Channel 6 Gain Error High Byte	Board dependent
0x3B	DAC Channel 6 Gain Error Low Byte	Board dependent
0x3C	DAC Channel 7 Gain Error High Byte	Board dependent
0x3D	DAC Channel 7 Gain Error Low Byte	Board dependent
0x3E	DAC Channel 8 Gain Error High Byte	Board dependent
0x3F	DAC Channel 8 Gain Error Low Byte	Board dependent

Table 3-11: Calibration Data Space Address Map

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	9050 10B5
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	118000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFFE1
0x1C	PCI Base Address 3 for Local Address Space 1				Y	FFFFFFC0
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	0227 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 48 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 4C 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 4-1 : PCI9030 Header

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FFE1
0x04	Local Address Space 1 Range	0x0FFF_FFC0
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Expansion ROM Range	0x0000_0000
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_0101
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_0000
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000
0x28	Local Address Space 0 Bus Region Descriptor	0x5141_2080
0x2C	Local Address Space 1 Bus Region Descriptor	0x5505_6280
0x30	Local Address Space 2 Bus Region Descriptor	0x0000_0000
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0009
0x40	Chip Select 1 Base Address	0x0000_0019
0x44	Chip Select 2 Base Address	0x0000_0121
0x48	Chip Select 3 Base Address	0x0000_0000
0x4C	Interrupt Control/Status	0x0041
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x807C_4000
0x54	General Purpose I/O Control	0x0000_0240
0x70	Hidden1 Register for Power Management Data Select	0x0000_0000
0x74	Hidden2 Register for Power Management Data Scale	0x0000_0000

Table 4-2 : PCI9030 Local Configuration Registers

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9050	0x10B5	0x0280	0x0000	0x1180	0x0001	0x0227	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x4801	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFFE1	0x0FFF	0xFFC0
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0101	0x0000	0x0000	0x0000	0x0000	0x0000	0x0009
0x50	0x5141	0x2080	0x5505	0x6280	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0009	0x0000	0x0019	0x0000	0x0121
0x70	0x0000	0x0000	0x0030	0x0041	0x807C	0x4000	0x0000	0x0240
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM

4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

5 Configuration Hints

5.1 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 5-1 : Local Bus Little/Big Endian

Standard use of the TPMC551:

Local Address Space 0	16 bit bus in Big Endian Mode
Local Address Space 1	8 bit bus in Big Endian Mode
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

For further information please refer to the PCI9030 manual which is also part of the TPMC551-ED Engineering Documentation.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut Offset	Name	
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers

6 Functional Description

6.1 DAC Data Coding

The following table shows the data coding for each output voltage range.

Data Value	Analog Output Voltage	
Voltage Range: 0 … 10V		
0xFFFF	+FSR	9.999847V
0x8001	Midscale +1LSB	5.000153V
0x8000	Midscale	5V
0x7FFF	Midscale -1LSB	4.999847V
0x0000	-FSR	0V
Voltage Range: -10V … +10V		
0x7FFF	+FSR	+9.999695V
0x0001	Midscale +1LSB	+0.000305V
0x0000	Midscale	0V
0xFFFF	Midscale -1LSB	-0.000305V
0x8000	-FSR	-10V

Table 6-1 : DAC Data Coding

6.2 DAC Initialization

To reset the DAC devices and to set the DAC analog outputs to a known reset value, the following commands have to be performed:

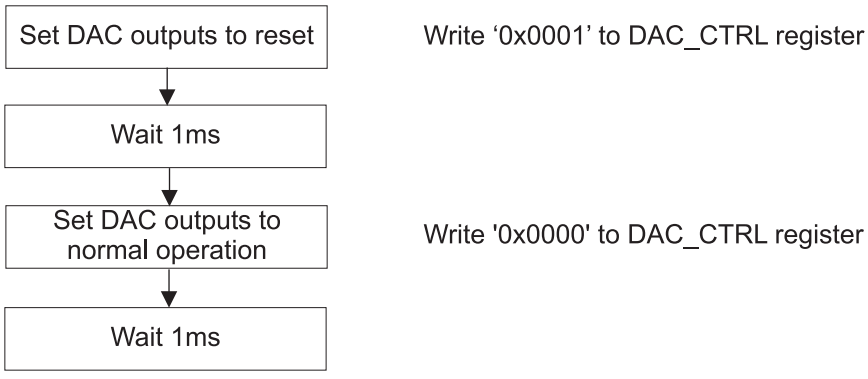

Figure 6-1 : Flowchart DAC Initialization

6.3 DAC Programming Modes

6.3.1 Conventional Mode

In conventional mode, the DAC operation is controlled by the following three registers: DAC Data Register (DAC_DATA), DAC Status Register (DAC_STAT) and DAC Convert Register (DAC_CONV). To perform a D/A conversion, this sequence has to be executed:

First, the data has to be written to the DAC_DATA register. Then, the DAC_BUSY (DBSY) bit in the DAC_STAT register has to be read as '0'. Afterwards, the desired output channel and conversion mode has to be selected by a write access to the DAC_CONV register. The actual conversion (or just the data transfer to the DAC internal registers, depending on the Load Mode) is started by the same write access.

The following figure presents the above mentioned steps as a flowchart:

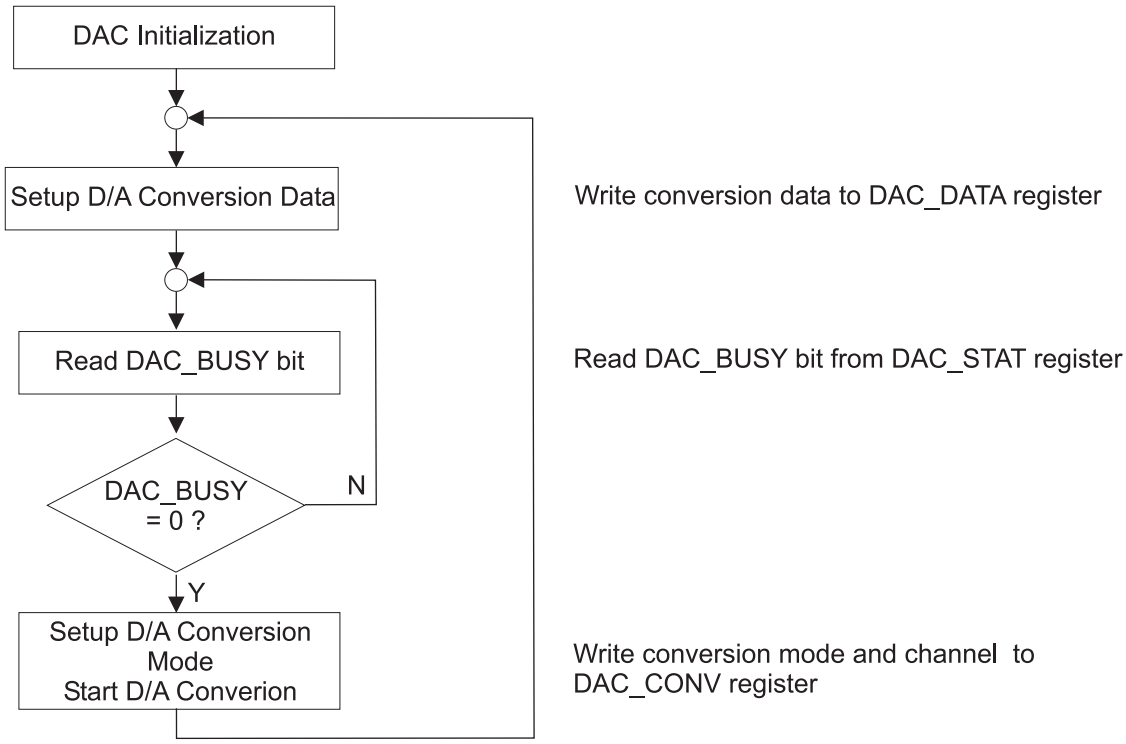

Figure 6-2 : Flowchart DAC Conventional Mode

6.3.1.1 Conventional Load Modes

In conventional mode, the DAC load mode is selected in the DAC_CONV register.

- In **Transparent Mode**, the D/A conversion loads the DAC internal channel register and immediately updates the analog output with the loaded value.
- In **Latched mode**, the D/A conversion only loads the DAC internal channel register without updating the analog output. This mode is used to load all DAC internal channel registers with independent data and afterwards update all channels at once with a separate simultaneous load command.

6.3.2 Sequencer Mode

In sequencer mode, the DAC operation is controlled by the following registers: Sequencer Control Register (SEQ_CTRL), Sequencer Status Register (SEQ_STAT), Sequencer Timer Register (SEQ_TIME) and also the Sequencer Data RAM. The sequencer mode is divided into two phases: Initialization and Running.

The initialization of the sequencer consists of these steps: First, the conversion data for the DAC channels has to be written into the Sequencer Data RAM. Then, the SEQ_STAT register has to be cleared to ensure a clean sequencer status. Optionally, the Sequencer Timer can be programmed through the SEQ_TIME register.

The running phase of the sequencer is started with a write access to the SEQ_CTRL register, which also sets up the channels, interrupt generation, runaround mode and load mode. Afterwards, the sequencer starts running. The user now has to wait until the sequencer sets the Sequencer Data Request (SDAT) bit inside the SEQ_STAT register. As soon as this bit is read as '1', the conversion data for the next sequencer has to be written to the Sequencer Data RAM. Even if the conversion data should be the same for the next sequence, the data has to be rewritten. Sequencer modes and enabled channels are changeable in the SEQ_CTRL register and do not affect the current sequence. The update of the Sequencer Data RAM and/or sequencer modes has to be confirmed by clearing the SDAT bit in the SEQ_STAT register. If the sequencer is ready to start the next sequence and the SDAT bit was not cleared yet, the sequencer sets the Sequencer Data Underflow (SUFL) bit inside the SEQ_STAT register to inform the user that a data underflow has occurred. However, the sequencer will not stop running. It will start the next sequence using the data values and settings from the previous sequence. To stop the sequencer, the SEQ_CTRL register has to be used.

Data underflows occur if the configured sequence takes less time to complete than the time needed to update the Sequencer Data RAM, the sequencer mode and channels and the confirmation of the SDAT bit combined.

The time of a complete sequence is approximately: #_of_D/A_Channels * 4.8µs. To extend the time of a sequence, the sequencer timer is available.

The sequencer mode is not intended for updating the D/A channels with a fast conversion rate. It is intended to update D/A channels with a fixed conversion rate.

6.3.2.1 Sequencer Runaround Modes

The sequencer runaround mode is selected in the SEQ_CTRL register.

- In **Continuous Mode**, the next sequence is immediately started after the sequencer is done.
- In **Timer Mode**, the sequencer waits until the sequencer timer expires before the next sequence is started. The sequencer timer value is set in the SEQ_TIME register. The timer step size is 100µs. A timer value of 0 effectively puts the sequencer into continuous mode. Future references to Timer Mode therefore assume timer values > 0. Timer values = 0 are covered by continuous mode.

6.3.2.2 Sequencer Load Modes

The sequencer load mode is selected in the SEQ_CTRL register.

- In **Transparent Mode**, each enabled DAC analog output is updated immediately after the DAC internal channel register is loaded within the sequence. This is valid for both continuous as well as timer runaround mode.
- In **Latched Mode**, all enabled DAC analog outputs are updated simultaneously at the end of a sequence. If the latched mode is selected in combination with the continuous runaround mode, all outputs are updated directly after all the DAC internal channel registers have been loaded with data. If selected in combination with the timer runaround mode, all outputs are updated as soon as the timer expires.

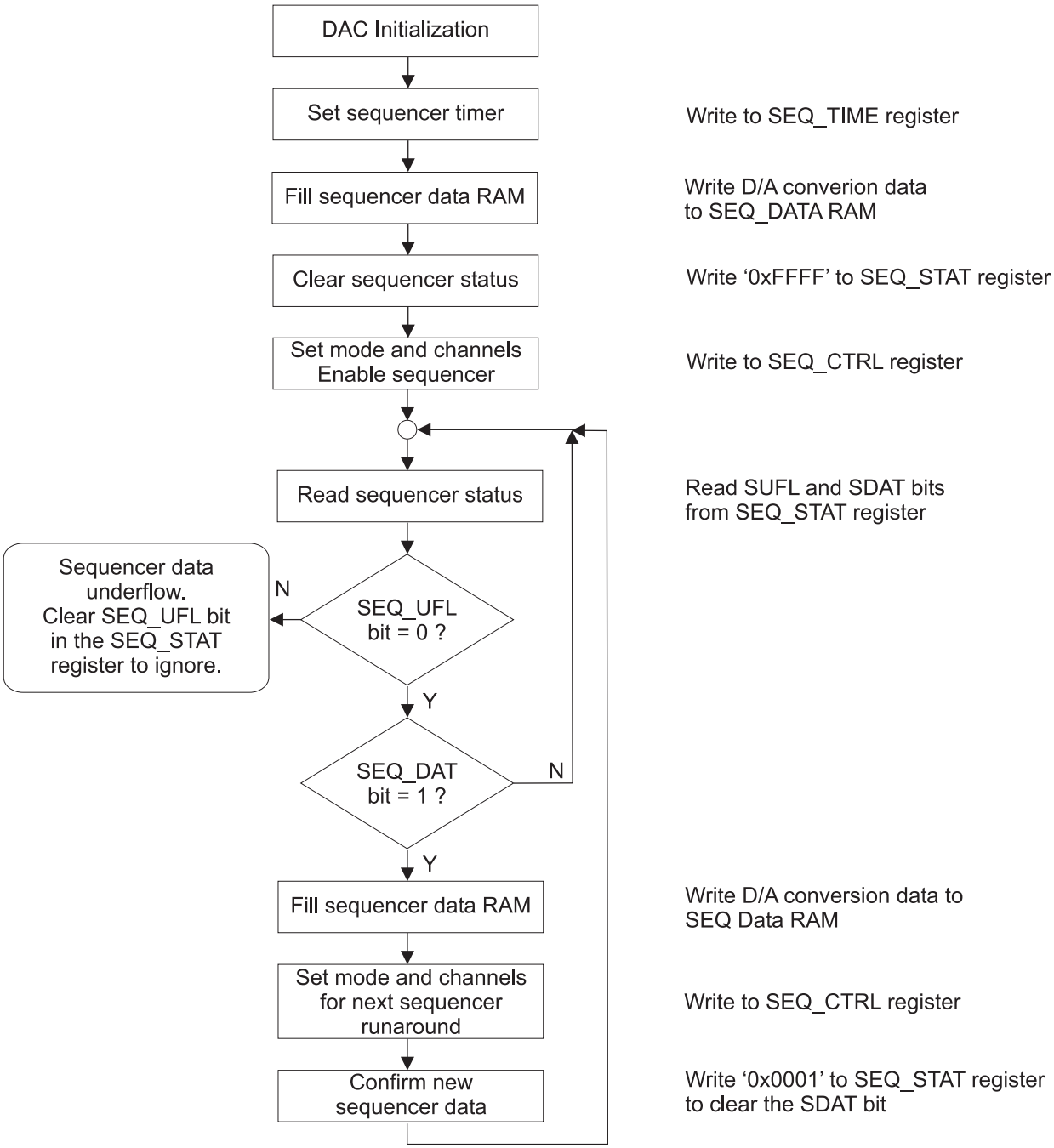

Figure 6-3 : Flowchart DAC Sequencer Mode

7 Programming Hints

7.1 DAC Data Correction

There are two errors affecting the accuracy of the DAC that can be corrected using the factory calibrated calibration data space.

First, there is the so called “offset error”. For the DAC, this is the data value that is required to produce a zero voltage output signal. This error is corrected by subtracting the offset from the DAC data value.

Second, there is the so called “gain error”. The gain error is the difference between the ideal gain and the actual gain of the DAC. It is corrected by multiplying the DAC data value with a correction factor.

The correction values are obtained during factory calibration and are stored in an on-board EEPROM as 2-complement byte-wide values in the range from -32768 to +32767. To achieve a higher accuracy, they are scaled to ¼LSB.

Floating point arithmetic or scaled integer arithmetic must be used to avoid rounding errors in computing above formula.

7.1.1 DAC Value Correction for 0V…10V Output Voltage Range

The basic formula for correcting the DAC output value in unipolar mode is:

$$Data = Value * (1 - GAIN_{corr} / 262144) - OFFSET_{corr} / 4$$

Data is the corrected digital value that should be programmed to the data register. *Value* is the ideal digital value for the desired output voltage. $GAIN_{corr}$ and $OFFSET_{corr}$ are the correction factors from the on board EEPROM. $GAIN_{corr}$ and $OFFSET_{corr}$ are stored separately for each of the possible D/A channels.

7.1.2 DAC Value Correction for ±10V Output Voltage Range

The basic formula for correcting DAC output value in bipolar mode is:

$$Data = Value * (1 - GAIN_{corr} / 131072) - OFFSET_{corr} / 4$$

Data is the corrected digital value that should be programmed to the data register. *Value* is the ideal digital value for the desired output voltage. $GAIN_{corr}$ and $OFFSET_{corr}$ are the correction factors from the on board EEPROM. $GAIN_{corr}$ and $OFFSET_{corr}$ are stored separately for each of the possible D/A channels.

The $GAIN_{corr}$ and $OFFSET_{corr}$ values can be read in the Calibration Data Space.

8 Installation

8.1 Solder Pads Configuration

Solder Pads	Function	Configuration	Option
LB1	Output Voltage Range D/A channels 1 to 4	1-2 closed	0…10V
		2-3 open	
		1-2 open	±10V
		2-3 closed	
LB2 (TPMC551-10 and TPMC551-20 only)	Output Voltage Range D/A channels 5 to 8	1-2 closed	0…10V
		2-3 open	
		1-2 open	±10V
		2-3 closed	

Table 8-1 : Solder Pads Configuration

Do not connect or solder all three pads together, only two of them at once!

8.2 Solder Pads Location

The following figure shows the location of the solder pads from the bottom view:

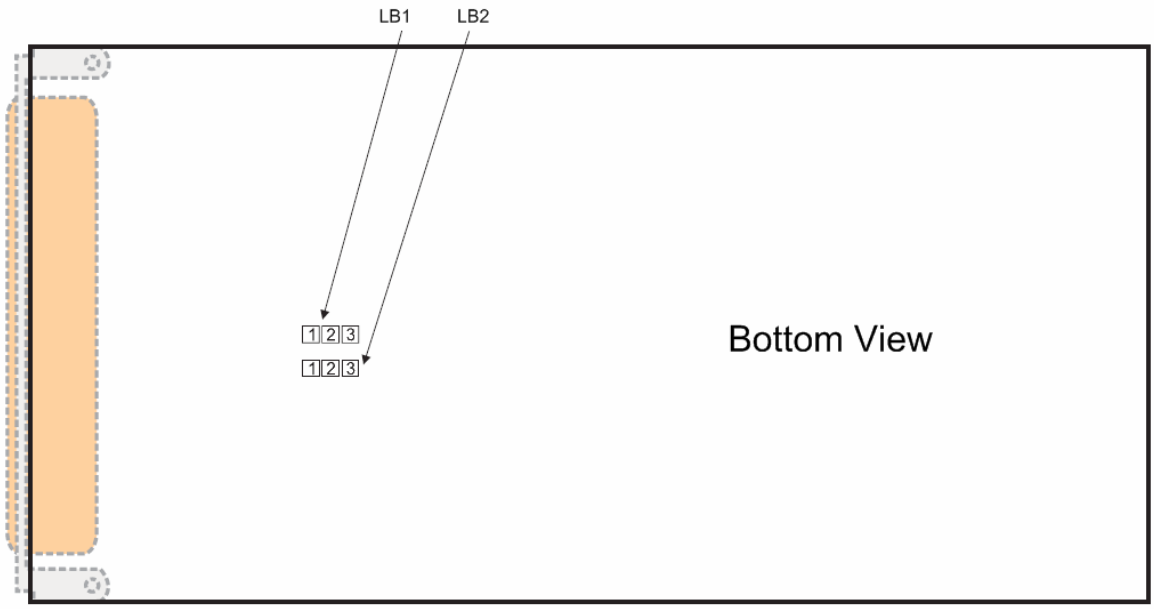

Figure 8-1 : Solder Pads Location (Bottom View)

9 Pin Assignment – I/O Connector

9.1 Front Panel I/O Connector

The front panel I/O connector applies for TPMC551-1x board options only.

Pin-Count	25
Connector Type	DB25 female connector (Harting part#: 0966 352 6616)

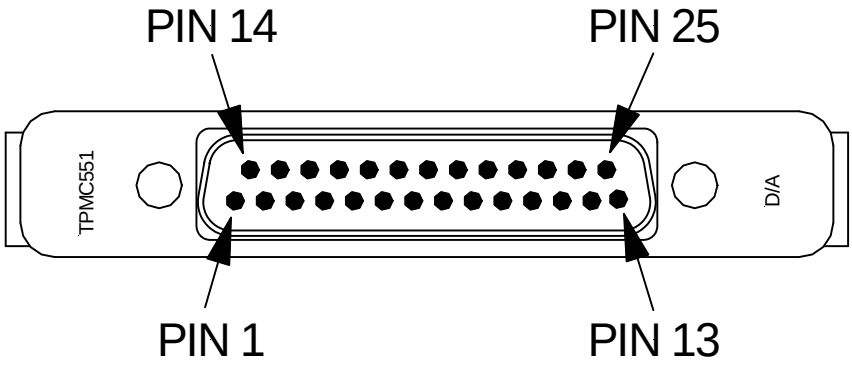

Figure 9-1 : Front Panel I/O Connector

9.1.1 Pin Assignment

Pin	Signal	Level
1	DAC_OUT_1	±10V
2	DAC_OUT_2	±10V
3	DAC_OUT_3	±10V
4	DAC_OUT_4	±10V
5	DAC_OUT_5	±10V
6	DAC_OUT_6	±10V
7	DAC_OUT_7	±10V
8	DAC_OUT_8	±10V
9	-	-
10	-	-
11	-	-
12	-	-
13	-	-

Pin	Signal	Level
14	AGND	
15	AGND	
16	AGND	
17	AGND	
18	AGND	
19	AGND	
20	AGND	
21	AGND	
22	-	-
23	-	-
24	-	-
25	-	-

Table 9-1 : Pin Assignment Front I/O Panel Connector

9.2 Back I/O PMC P14 Connector

The P14 mezzanine back I/O connector applies for TPMC551-2x board options only.

9.2.1 Pin Assignment

Pin	Signal	Level / Description
1	DAC_OUT_1	D/A output channel 1
2	AGND	Signal ground for D/A output channels
3	DAC_OUT_2	D/A output channel 2
4	AGND	Signal ground for D/A output channels
5	DAC_OUT_3	D/A output channel 3
6	AGND	Signal ground for D/A output channels
7	DAC_OUT_4	D/A output channel 4
8	AGND	Signal ground for D/A output channels
9	DAC_OUT_5	D/A output channel 5 (TPMC550-20 only)
10	AGND	Signal ground for D/A output channels
11	DAC_OUT_6	D/A output channel 6 (TPMC550-20 only)
12	AGND	Signal ground for D/A output channels
13	DAC_OUT_7	D/A output channel 7 (TPMC550-20 only)
14	AGND	Signal ground for D/A output channels
15	DAC_OUT_8	D/A output channel 8 (TPMC550-20 only)
16	AGND	Signal ground for D/A output channels
17		
…		
64		

Table 9-2 : Pin Assignment PMC P14 I/O Connector