The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC553

32 / 16 Channels of 16 bit D/A

Version 1.0

User Manual

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7
25469 Halstenbek, Germany
www.tews.com
Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TEWS TECHNOLOGIES LLC
9190 Double Diamond Parkway,
Suite 127, Reno, NV 89521, USA
www.tews.com
Phone: +1 (775) 850 5830
Fax: +1 (775) 201 0347
e-mail: usasales@tews.com

TPMC553-10

32 Channels of 16 bit D/A

TPMC553-11

16 Channels of 16 bit D/A

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Initial Issue	September 2008
1.1	Revised DAC correction section	October 2008
1.0.2	New Notation for User Manual and Engineering Documentation	March 2009

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1 Product Description

The TPMC553 is a standard single-wide 32 bit PMC module and provides 32/16 channels of 16 bit analog outputs. All signals are accessible through a HD68 SCSI-3 type front I/O connector.

The software selectable output voltage ranges are 0-5V, 0-10V, 0-10.8V, ±5V, ±10V or ±10.8V. The output voltage range can be individually set per channel. The conversion time is typ. 10 µs and the DAC outputs are capable to drive a load of 2kΩ, with a capacitance up to 4000pF.

Beside of an individual channel update, the double buffered DACs allow simultaneous update of all channels. Additionally a sequencer on the TPMC553 allows to periodically updating enabled channels with a sequence timer range that extends from 10µs to 167s.

Each TPMC553 is factory calibrated. The calibration information is stored in an on board serial EEPROM unique to each PMC module.

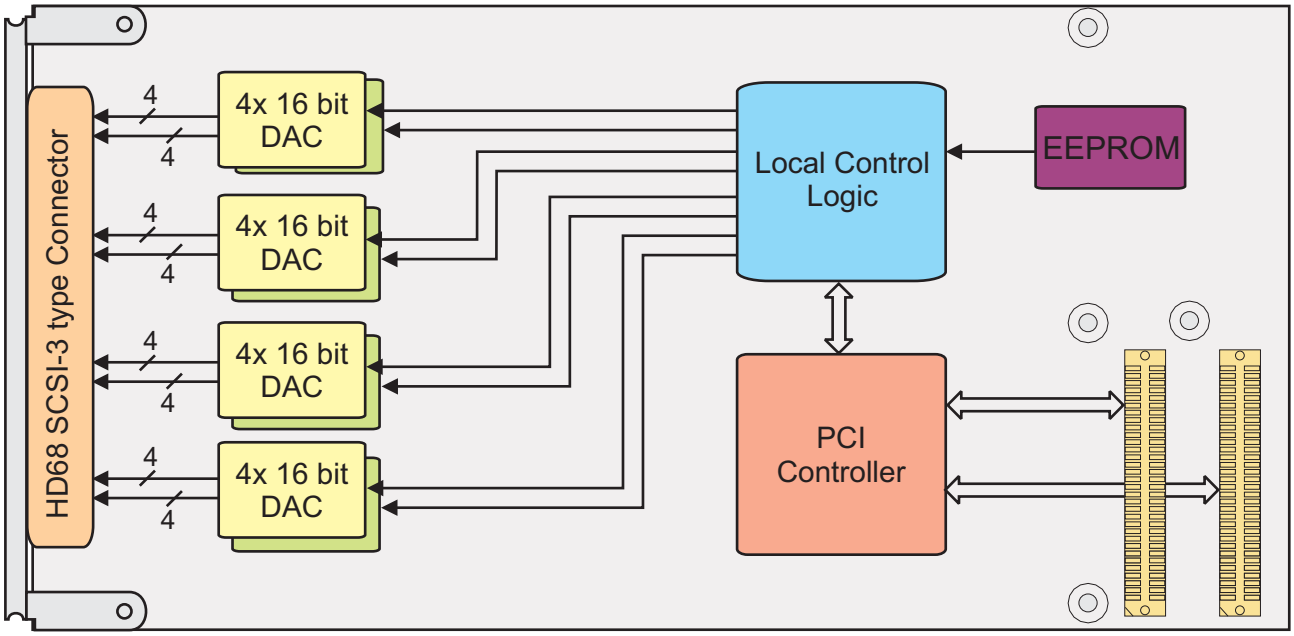

Figure 1-1: Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9030 (PLX Technology)	
Quad-DAC	AD5754R (Analog Devices)	
I/O Interface		
Number of D/A Channels	TPMC553-10: 32 D/A channels TPMC553-11: 16 D/A channels	
D/A Resolution	16 bit	
D/A Output Voltage Range	Selectable: 0V - +5V, 0V - +10V, 0V - +10.8V, ±5V, ±10V, ±10.8V	
D/A Channel Load	Max 2kΩ | 4000pF per D/A channel	
D/A Channel Settling Time	Max 10us	
D/A Protection	20mA current limit option, thermal shutdown option	
D/A Calibration	Calibration data for gain and offset correction	
DAC INL/DNL Error	±16/±1 LSB	
I/O Connector	Front I/O HD68 / SCSI-3 (AMP 5-787082-7 or compatible)	
Physical Data		
Power Requirements	200mA typical @ 3.3V 600mA typical @ 5V (±10V output, 2kΩ load)	
Temperature Range	Operating Storage	-40°C - +85°C -40°C - +85°C
MTBF	TPMC553-10: 683000 h TPMC553-11: 689000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	79 g	

Table 2-1 : Technical Specification

3 General Notes on the TPMC553 Quad-DACs

The TPMC553 is using Quad-DAC (Q-DAC) devices. Each Q-DAC device provides four D/A channels, internally called A, B, C and D.

The TPMC553-10 provides 32 D/A channels (1 to 32), thus eight Q-DAC devices (1 to 8). The TPMC553-11 provides 16 D/A channels (1 to 16), thus four Q-DAC devices (1 to 4).

The Q-DAC device provides an internal data register for each of the four D/A channels.

To set a certain analog output voltage, the D/A channel data is written to a DAC Data Space, from where it is transferred to the appropriate Q-DAC internal D/A channel data register automatically as soon as possible. The Q-DAC analog outputs are then updated, depending on the Q-DAC operating mode used.

Each Q-DAC devices provides a single serial interface, so all transfers to the Q-DACs are in fact serial data transfers. A data transfer to a Q-DAC takes approx. 1.4us per D/A channel, data transfer for all four Q-DAC D/A channels takes approx. 5.6us. A Q-DAC status read takes approx. 3.4us.

The Q-DAC data transfer engines (parallel/serial) are independent of each other (e.g. data for D/A channels 1, 2, 3 & 4 is transferred one channel after the other since these channels are located in the same Q-DAC, while data for D/A channels 1, 5, 9, 13 could be transferred all at the same time since these channels are located in different Q-DACs.

TPMC553 D/A Channel	Q-DAC	Q-DAC internal D/A Channel
1	1	A
2		B
3		C
4		D
5	2	A
6		B
7		C
8		D
9	3	A
10		B
11		C
12		D
13	4	A
14		B
15		C
16		D
17	3	A
18		B
19		C
20		D
21	6	A
22		B
23		C
24		D

TPMC553 D/A Channel	Q-DAC	Q-DAC internal D/A Channel
25	7	A
26		B
27		C
28		D
29	8	A
30		B
31		C
32		D

Table 3-1 : D/A Channel to Q-DAC mapping

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	0229 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	118000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFE00
0x1C	PCI Base Address 3 for Local Address Space 1				Y	FFFFFFC0
0x20	PCI Base Address 4 for Local Address Space 2				Y	FFFFFC00
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	s.b. 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 48 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 4C 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 4-1 : PCI9030 Header

Subsystem-ID: TPMC553-10 (32 Channels of 16 bit D/A) = 0x000A

TPMC553-11 (16 Channels of 16 bit D/A) = 0x000B

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from an on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0xFFFFFE00
0x04	Local Address Space 1 Range	0xFFFFFFC0
0x08	Local Address Space 2 Range	0xFFFFFC00
0x0C	Local Address Space 3 Range	0x00000000
0x10	Expansion ROM Range	0x00000000
0x14	Local Address Space 0 Local Base Address (Remap)	0x00000001
0x18	Local Address Space 1 Local Base Address (Remap)	0x00010001
0x1C	Local Address Space 2 Local Base Address (Remap)	0x00020001
0x20	Local Address Space 3 Local Base Address (Remap)	0x00000000
0x24	Expansion ROM Local Base Address (Remap)	0x00000000
0x28	Local Address Space 0 Bus Region Descriptor	0xD180A0E0
0x2C	Local Address Space 1 Bus Region Descriptor	0xD180A0E0
0x30	Local Address Space 2 Bus Region Descriptor	0xD180A0E0
0x34	Local Address Space 3 Bus Region Descriptor	0x00000000
0x38	Expansion ROM Bus Region Descriptor	0x00000000
0x3C	Chip Select 0 Base Address	0x00000101
0x40	Chip Select 1 Base Address	0x00010041
0x44	Chip Select 2 Base Address	0x00020401
0x48	Chip Select 3 Base Address	0x00000000
0x4C	Interrupt Control/Status	0x0041
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x00780000
0x54	General Purpose I/O Control	0x00392270
0x70	Hidden1 Register for Power Management Data Select	0x00000000
0x74	Hidden 2 Register for Power Management Data Scale	0x00000000

Table 4-2 : PCI9030 Local Configuration Registers

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from an on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0229	0x1498	0x0280	0x0000	0x1180	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFE00	0x0FFF	0xFFC0
0x30	0x0FFF	0xFC00	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0001	0x0001	0x0002	0x0001	0x0000	0x0000	0x0000	0x0000
0x50	0xD180	0xA0E0	0xD180	0xA0E0	0xD180	0xA0E0	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0101	0x0001	0x0041	0x0002	0x0401
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x0000	0x0039	0x2270
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM TPMC553-1x

Subsystem-ID Value (Offset 0x0C): TPMC553-10 0x000A

TPMC553-11 0x000B

4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

5 Local Space Addressing

5.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	512	32	BIG	Register Space
1	3 (0x1C)	MEM	64	32	BIG	DAC Data Space
2	4 (0x20)	MEM	1K	32	BIG	Calibration Data Space
3	5 (0x24)	-	-	-	-	Not Used

Table 5-1 : PCI9030 Local Space Configuration

5.2 Register Space

PCI Base Address: PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).

Offset to PCI Base Address 2	Description	Size (Bit)
0x000	Q-DAC 1 Configuration Register	32
0x004	Q-DAC 2 Configuration Register	32
0x008	Q-DAC 3 Configuration Register	32
0x00C	Q-DAC 4 Configuration Register	32
0x010	Q-DAC 5 Configuration Register	32
0x014	Q-DAC 6 Configuration Register	32
0x018	Q-DAC 7 Configuration Register	32
0x01C	Q-DAC 8 Configuration Register	32
0x020	Q-DAC 1 Control Register	32
0x024	Q-DAC 2 Control Register	32
0x028	Q-DAC 3 Control Register	32
0x02C	Q-DAC 4 Control Register	32
0x030	Q-DAC 5 Control Register	32
0x034	Q-DAC 6 Control Register	32
0x038	Q-DAC 7 Control Register	32
0x03C	Q-DAC 8 Control Register	32
0x040	Q-DAC 1 Status Register	32
0x044	Q-DAC 2 Status Register	32

Offset to PCI Base Address 2	Description	Size (Bit)
0x048	Q-DAC 3 Status Register	32
0x04C	Q-DAC 4 Status Register	32
0x050	Q-DAC 5 Status Register	32
0x054	Q-DAC 6 Status Register	32
0x058	Q-DAC 7 Status Register	32
0x05C	Q-DAC 8 Status Register	32
0x060	Q-DAC 1 Sequencer Timer Register	32
0x064	Q-DAC 2 Sequencer Timer Register	32
0x068	Q-DAC 3 Sequencer Timer Register	32
0x06C	Q-DAC 4 Sequencer Timer Register	32
0x070	Q-DAC 5 Sequencer Timer Register	32
0x074	Q-DAC 6 Sequencer Timer Register	32
0x078	Q-DAC 7 Sequencer Timer Register	32
0x07C	Q-DAC 8 Sequencer Timer Register	32
0x080	Clear Register	32
0x084	Load Register	32
0x088	Global Control Register	32
0x08C	Global Status Register	32
0x090	Interrupt Status Register	32
0x094	Auto Status Timer Register	32

Table 5-2 : Register Space Address Map

The Register Space requires using 32 bit transfer size.

Registers / Register bits for Q-DACs 5 - 8 are supported for 32 D/A channel TPMC553 options only.

5.2.1 Q-DAC X Configuration Register (X = 1-8) (Offset 0x00 …)

There is a dedicated Q-DAC Configuration Register for each Q-DAC.

Each Q-DAC provides four D/A Channels, internally called A - D. Each Q-DAC also provides internal registers for device configuration.

If the Q-DAC busy bit in the Global Status Register is clear, a write to a Q-DAC Configuration Register starts the Q-DAC configuration (i.e. the Q-DAC configuration register setting is transferred to the Q-DAC internal configuration registers). Each Q-DAC configuration sequence does also include a read of the Q-DAC status (see Q-DAC Status Register).

Check the Q-DAC busy bit in the Global Status Register to determine when the Q-DAC configuration is done.

Each Q-DAC that is used must be configured first. A D/A Channel can only be used if it's PUA-bit is set.

Writes to a Q-DAC Configuration Register are ignored, when the Q-DAC busy bit is set in the Global Status Register.

Bit	Symbol	Description	Access	Reset Value
31:20	-	Reserved Set '0' for writes, undefined for reads.	-	-
19	PUD	D/A Channel D Power-Up See PUA description.	R/W	0
18	PUC	D/A Channel C Power-Up See PUA description.	R/W	0
17	PUB	D/A Channel B Power-Up See PUA description.	R/W	0
16	PUA	D/A Channel A Power-Up. When set, this bit places DAC A in normal operating mode. When cleared, this bit places DAC A in power-down mode (default).	R/W	0
15	TSD ENA	TSD Enable Set to enable the Q-DAC thermal shutdown feature. Cleared to disable the thermal shutdown feature (default). The Q-DAC incorporates a thermal shutdown feature that automatically shuts down the device if the max device temperature is exceeded.	R/W	0
14	CL ENA	Clamp Enable Set to enable the current limit clamp (default). The channel current is clamped at 20mA in case of over-current. Clear to disable the current-limit clamp. The channel powers down in case of over-current.	R/W	1

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>13</td><td>CLR SEL</td><td>Q-DAC Clear Select
Selects the D/A Channel default values in case the Q-DAC is cleared using the Clear Register.

<table><tr><th>CLR SEL</th><th>Unipolar Output Range</th><th>Bipolar Output Range</th></tr><tr><td>0</td><td>0V</td><td>0V</td></tr><tr><td>1</td><td>Mid-scale</td><td>Negative Full-scale</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>12</td><td>-</td><td>Reserved
Set '0' for writes, undefined for reads.</td><td>-</td><td>-</td></tr>
<tr><td>11:9</td><td>ORD</td><td>D/A Channel D Output Range
See ORA description.</td><td>R/W</td><td>000</td></tr>
<tr><td>8:6</td><td>ORC</td><td>D/A Channel C Output Range
See ORA description.</td><td>R/W</td><td>000</td></tr>
<tr><td>5:3</td><td>ORB</td><td>D/A Channel B Output Range
See ORA description.</td><td>R/W</td><td>000</td></tr>
<tr><td>2:0</td><td>ORA</td><td>D/A Channel A Output Range

<table><tr><th>ORA</th><th>Output Voltage Range</th></tr><tr><td>000</td><td>+5V</td></tr><tr><td>001</td><td>+10V</td></tr><tr><td>010</td><td>+10.8V</td></tr><tr><td>011</td><td>±5V</td></tr><tr><td>100</td><td>±10V</td></tr><tr><td>101</td><td>±10.8V</td></tr><tr><td>others</td><td>reserved</td></tr></table></td><td>R/W</td><td>000</td></tr>
</table>

Table 5-3 : Q-DAC Configuration Register (Offset 0x00 …)

5.2.2 Q-DAC X Control Register (X = 1-8) (Offset 0x20 …)

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved Set '0' for writes, undefined for reads.	-	-
9	RDSTA	Read Q-DAC Status Register Only valid for I-Mode and M-Mode (ignored for other QDAC modes). When set, a request for reading the Q-DAC status is logged and the status valid bit in the Q-DAC Status Register is cleared. When the Q-DAC status read is done, the Q-DAC status register is updated and the status valid bit is set again. The actual Q-DAC status read may be delayed by ongoing processes. Bit clears immediately.	W	0
8	GLM	Enable Global Load Mode for this Q-DAC Used in M-Mode only. When set, this QDAC operates in global load mode. In global load mode, all four analog outputs of the Q-DAC are updated simultaneously along with the analog outputs of other Q-DACs set to global load mode when all available D/A channel data has been transferred to the Q-DACs. When clear, this QDAC operates in standalone mode. In standalone mode, all four analog outputs of the Q-DAC are updated simultaneously when all available D/A channel data has been transferred to the Q-DAC.	R/W	0
7	ASR	Automatic Status Read Could be used for I-Mode, M-Mode and T-Mode. Set to enable automatic status reads of the Q-DAC internal status register. Clear to disable automatic status reads. See Auto Status Timer Register for I-Mode and M-Mode. In T-Mode (if enabled) there is one automatic Q-DAC status read per sequence (approx. 10us after the previous Q-DAC update).	R/W	0
6	-	Reserved Set '0' for writes, undefined for reads.	-	-
5	IRQSE	Q-DAC Sequencer IRQ enable. Enables Q-DAC Sequencer interrupts when set. Disables Q-DAC Sequencer interrupts when clear. See Interrupt Status Register for details.	R/W	0
4	IRQAL	Q-DAC Alert IRQ enable. Enables Q-DAC Alert interrupts when set. Disables Q-DAC Alert interrupts when clear. See Interrupt Status Register for details.	R/W	0
3	IRQLD	Q-DAC Load IRQ enable Enables Q-DAC Load interrupt when set. Disables Q-DAC Load interrupts when clear. Should be disabled for I-Mode and T-Mode. See Interrupt Status Register for details.	R/W	0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>2:0</td><td>MODE</td><td>Q-DAC Mode

<table>
<tr><th>MODE</th><th>Q-DAC Mode</th><th>Description</th></tr>
<tr><td>000</td><td>I-Mode</td><td>Instant Mode
Q-DAC analog outputs are updated immediately after each D/A Channel data transfer</td></tr>
<tr><td>001</td><td>M-Mode</td><td>Manual Mode
Q-DAC analog outputs are updated simultaneously per software command. D/A Channel data has been transferred to the Q-DAC before.</td></tr>
<tr><td>010</td><td>-</td><td>Reserved</td></tr>
<tr><td>011</td><td>T-Mode</td><td>Timer Mode
An internal sequencer timer triggers the data transfer to the Q-DAC and the simultaneous update of the Q-DAC analog outputs.</td></tr>
<tr><td>1xx</td><td>-</td><td>Reserved</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
</table>

Table 5-4 : Q-DAC Control Register (Offset 0x20 …)

5.2.3 Q-DAC X Status Register (X = 1-8) (Offset 0x40 …)

The Q-DACs device used provides an internal status register, which is reflected in the Q-DAC X Status Registers. The Q-DAC X Status Registers are only updated when a status register read is ordered by writing a ‘1’ to the RDSTA bit or the when ASR option is active.

Bit	Symbol	Description	Access	Reset Value
31:11	-	Reserved Set '0' for writes, undefined for reads.	-	-
10	SVAL	Status is valid This bit indicates that the other register bits are showing the result of a Q-DAC status read (no random data). It does not necessarily indicate that the other register bits are showing the most current Q-DAC status. This bit is automatically set after the first Q-DAC status read (e.g. during Q-DAC configuration). The bit is cleared upon a Q-DAC status read request via the Q-DAC control register in I-Mode or M-Mode. The bit is then automatically set again, when the requested Q-DAC status read is done.	R	0
9	TSD	Thermal Shutdown Alert In the event of an over-temperature situation, this bit is set.	R	0
8	PUREF	Reference Power-Up When set, this bit indicates that the Quad-DAC internal reference is powered-up. Since the TPMC553 Quad-DACs are operating with internal reference, this bit should always be set for any status read from the Quad-DAC.	R	0
7	PUD	DAC D Power-Up See PUA description.	R	0
6	PUC	DAC C Power-Up See PUA description.	R	0
5	PUB	DAC B Power-Up See PUA description.	R	0
4	PUA	DAC A Power-Up ‘0’ when powered down, ‘1’ when powered up. If the Q-DAC is configured with CL ENA bit clear, DAC A will power down automatically on detection of an over-current, PUA will be cleared to reflect this.	R	0
3	OCD	DAC D Over-current Alert See OCA description.	R	0
2	OCC	DAC C Over-current Alert See OCA description.	R	0
1	OCB	DAC B Over-current Alert See OCA description.	R	0
0	OCA	DAC A Over-current Alert In the event of an over-current situation on DAC A, this bit is set.	R	0

Table 5-5 : Q-DAC Status Register (Offset 0x40 …)

5.2.4 Q-DAC X Sequencer Timer Register (X = 1-8) (Offset 0x60 …)

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved Set '0' for writes, undefined for reads.	-	-
23:0	STPV	Sequencer Timer Preload Value Controls the time between consecutive Q-DAC analog output updates in T-Mode. Actual time between consecutive Q-DAC analog output updates is (STPV + 1) x 10us.	R/W	0

Table 5-6 : Q-DAC Sequencer Timer Register (Offset 0x60 …)

5.2.5 Clear Register (Offset 0x80)

The Clear Register can be used to clear the 4 channels of a specific Q-DAC or to perform a global clear.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved Set '0' for writes, undefined for reads.	-	-
7	CLR8	There is one clear control bit for each Q-DAC. When set, the Q-DAC clear signal is asserted. Could be used to set all four Q-DAC channels (internal D/A Channel registers and analog outputs) to a value specified by the Q-DACs CLR SEL setting (see Q-DAC Configuration Register).	R/W	0
6	CLR7		R/W	0
5	CLR6		R/W	0
4	CLR5		R/W	0
3	CLR4		R/W	0
2	CLR3		R/W	0
1	CLR2		R/W	0
0	CLR1		R/W	0

Table 5-7 : Clear Register (Offset 0x80)

Do not change the output voltage range while the Q-DAC clear signal is active, as this might put the analog outputs to a value other than 0V.

5.2.6 Load Register (M-Mode) (Offset 0x84)

The Load Register is used to load (=update) the four analog outputs of a specific Q-DAC in M-Mode.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved Set '0' for writes, undefined for reads.	-	-
7	LOAD8	Q-DAC Analog Output Update Request. There is one load control/status bit for each Q-DAC. Only valid for M-Mode (ignored for other Q-DAC modes). When set, a request is logged to update the Q-DAC analog outputs. When the request has been logged, the Q-DAC analog outputs are updated when all available D/A Channel data for this Q-DAC has been transferred to the Q-DAC internal data registers. If the Q-DAC is configured for Global-M-Mode, the update of the Q-DAC analog outputs is delayed until all Q-DACs in Global-M-Mode are ready for updating their analog outputs simultaneously. The bit is automatically cleared when the Q-DAC analog outputs are actually updated.	R/W	0
6	LOAD7		R/W	0
5	LOAD6		R/W	0
4	LOAD5		R/W	0
3	LOAD4		R/W	0
2	LOAD3		R/W	0
1	LOAD2		R/W	0
0	LOAD1		R/W	0

Table 5-8 : Load Register (M-Mode) (Offset 0x84)

In M-Mode, after setting a LOAD-bit, software shall check that this bit is clear, before new DAC data for this Q-DAC is written to the DAC data space (since, once written to the DAC data space, the data is transferred to the Q-DAC as soon as possible and may interfere with an ongoing update of the analog outputs).

5.2.7 Global Control Register (Offset 0x88)

Bit	Symbol	Description	Access	Reset Value
31:9	-	Reserved Set '0' for writes, undefined for reads.	-	-
8	MIE	Master Interrupt Enable '0': Interrupts are disabled '1': Interrupts are enabled There are also dedicated enable/disable bits for the various interrupt sources. See Q-DAC Control Register.	R/W	0
7	SEQST8	Q-DAC Sequencer Start/Stop There is one Sequencer Start/Stop bit for each Q-DAC. 0 : Stop Sequencer 1 : Start Sequencer When the sequencer is running, the Q-DAC busy bit in the global status register is permanently set. When the sequencer is stopped, any Q-DAC data transfer in progress will terminate normally. Check the Q-DAC busy bit in the Global Status Register to determine when the sequencer is actually stopped. For a simultaneous update of the analog outputs of multiple Q-DACs in T-Mode, set the Q-DAC timer registers to the same value and start the sequencers using a single write access.	R/W	0
6	SEQST7		R/W	0
5	SEQST6		R/W	0
4	SEQST5		R/W	0
3	SEQST4		R/W	0
2	SEQST3		R/W	0
1	SEQST2		R/W	0
0	SEQST1		R/W	0

Table 5-9 : Global Control Register (Offset 0x88)

Prior a sequencer start, the following steps are required:

1. Setup the Q-DAC Timer

2. Set the Q-DAC Mode to T-Mode

3. Write the Q-DAC data for the first sequence to the DAC data space.

5.2.8 Global Status Register (Offset 0x8C)

Bit	Symbol	Description	Access	Reset Value
31	SDU8	Q-DAC 8 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
30	SDR8		R/C	0
29	SET8		R	0
28	BUSY8		R	0
27	SDU7	Q-DAC 7 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
26	SDR7		R/C	0
25	SET7		R	0
24	BUS7		R	0
23	SDU6	Q-DAC 6 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
22	SDR6		R/C	0
21	SET6		R	0
20	BUSY6		R	0
19	SDU5	Q-DAC 5 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
18	SDR5		R/C	0
17	SET5		R	0
16	BUSY5		R	0
15	SDU4	Q-DAC 4 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
14	SDR4		R/C	0
13	SET4		R	0
12	BUSY4		R	0
11	SDU3	Q-DAC 3 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
10	SDR3		R/C	0
9	SET3		R	0
8	BUSY3		R	0
7	SDU2	Q-DAC 2 status bits. (Refer to the Q-DAC 1 status bits for description).	R/C	0
6	SDR2		R/C	0
5	SET2		R	0
4	BUSY2		R	0
3	SDU1	Q-DAC 1 Sequencer Data Underflow Bit is set when the sequencer reads the D/A Channel data for the next sequence in T-Mode, but the software has not yet confirmed new D/A Channel data by clearing the Sequencer Data Request/Acknowledge bit. The sequencer continues normally and takes the D/A channel data actually found in the DAC Data Space. The bit is cleared by writing a '1'.	R/C	1
2	SDR1	Q-DAC 1 Sequencer Data Request/Acknowledge Bit is set when the sequencer is requesting new D/A Channel data for the next sequence in T-Mode. The bit is cleared by writing a '1'.	R/C	0

Bit	Symbol	Description	Access	Reset Value
1	SET1	Q-DAC 1 Settle Indicates Q-DAC analog output settling time. '1' when Q-DAC analog outputs are settling, '0' when Q-DAC analog outputs are stable. This is no physical representation of any kind, just an internal timer that expires 10µs after an update of the Q-DAC analog outputs.	R	0
0	BUSY1	Q-DAC 1 Busy Set in the following cases: (a) Transfer to the Q-DAC is in progress (configuration data transfer or D/A channel data transfer or status read transfer). Note for I-Mode and M-Mode: Data may be written to the DAC data space while a Q-DAC transfer is in progress. E.g. data for D/A channels 3 & 4 may be written to the DAC data space while the data for D/A channel 1 is actually being transferred to the Q-DAC and thus the busy bit is set. (b) Waiting for actual Q-DAC load in M-Mode (after a load request) (c) Sequencer is running Clear when Q-DAC control logic is in Idle state.	R	0

Table 5-10: Global Status Register (Offset 0x8C)

When the SDR-bit is set, software should write new data for this Q-DAC to the DAC Data Space. When the D/A Channel data for this Q-DAC has been written, software shall clear this bit to acknowledge the request.

5.2.9 Interrupt Status Register (Offset 0x90)

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved Set '0' for writes, undefined for reads.	-	-
23	IRQSE8	Q-DAC Sequencer Interrupt There is one Sequencer Interrupt bit for each Q-DAC. Set when the sequencer logic requests a new D/A Channel data set for the next sequence and the interrupt is enabled. Write '1' to clear the interrupt status bit. See Q-DAC Control Register for interrupt enable/disable control.	R/C	0
22	IRQSE7		R/C	0
21	IRQSE6		R/C	0
20	IRQSE5		R/C	0
19	IRQSE4		R/C	0
18	IRQSE3		R/C	0
17	IRQSE2		R/C	0
16	IRQSE1		R/C	0
15	IQRLD8	Q-DAC Load Interrupt There is one Load Interrupt bit for each Q-DAC. Set when Q-DAC has actually been loaded in M-Mode (Q-DAC analog outputs just have been updated) and the interrupt is enabled. Write '1' to clear the interrupt status bit. This interrupt should be disabled for other modes than M-Mode. See Q-DAC Control Register for interrupt enable/disable control.	R/C	0
14	IQRLD7		R/C	0
13	IQRLD6		R/C	0
12	IQRLD5		R/C	0
11	IQRLD4		R/C	0
10	IQRLD3		R/C	0
9	IQRLD2		R/C	0
8	IQRLD1		R/C	0
7	IRQAL8	Q-DAC Alert Interrupt There is one Alert Interrupt bit for each Q-DAC. Set when the Q-DAC status is read and any of the over-current bits or the thermal alert bit is set and the interrupt is enabled. Write '1' to clear the interrupt status bit. See Q-DAC Control Register for interrupt enable/disable control.	R/C	0
6	IRQAL7		R/C	0
5	IRQAL6		R/C	0
4	IRQAL5		R/C	0
3	IRQAL4		R/C	0
2	IRQAL3		R/C	0
1	IRQAL2		R/C	0
0	IRQAL1		R/C	0

Table 5-11: Interrupt Status Register (Offset 0x90)

For an interrupt status bit to be set, the interrupt must be enabled prior to the interrupt event.

An interrupt is asserted if the Master Interrupt Enable bit is set in the Global Control Register and there is at least one bit set in the Interrupt Status Register.

5.2.10 Auto Status Timer Register (Offset 0x94)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:28</td><td>ASRT8</td><td rowspan="7">Q-DAC Automatic Status Read Timer
There is one Automatic Status Read Timer bit for each Q-DAC.
Only valid if the ASR bit is set for Q-DAC 1 (Q-DAC 1 Control Register) and only valid for I-Mode and M-Mode.
In Auto Status Read Mode a request for reading the Q-DAC status is logged every ASRTx time. Any ongoing transfer of D/A channel data will be terminated normally before the Q-DAC status read transfer is started.</td><td>R/W</td><td>1000</td></tr>
<tr><td>27:24</td><td>ASRT7</td><td>R/W</td><td>1000</td></tr>
<tr><td>23:20</td><td>ASRT6</td><td>R/W</td><td>1000</td></tr>
<tr><td>19:16</td><td>ASRT5</td><td>R/W</td><td>1000</td></tr>
<tr><td>15:12</td><td>ASRT4</td><td>R/W</td><td>1000</td></tr>
<tr><td>11:8</td><td>ASRT3</td><td>R/W</td><td>1000</td></tr>
<tr><td>7:4</td><td>ASRT2</td><td>R/W</td><td>1000</td></tr>
<tr><td>3:0</td><td>ASRT1</td><td>
<table>
<tr><th>ASRT1</th><th>Time</th></tr>
<tr><td>0000</td><td>10us</td></tr>
<tr><td>0001</td><td>20us</td></tr>
<tr><td>0010</td><td>40us</td></tr>
<tr><td>0011</td><td>80us</td></tr>
<tr><td>0100</td><td>160us</td></tr>
<tr><td>0101</td><td>320us</td></tr>
<tr><td>0110</td><td>640us</td></tr>
<tr><td>0111</td><td>1.280ms</td></tr>
<tr><td>1000</td><td>2.560ms</td></tr>
<tr><td>1001</td><td>5.120ms</td></tr>
<tr><td>1010</td><td>10.240ms</td></tr>
<tr><td>1011</td><td>20.480ms</td></tr>
<tr><td>1100</td><td>40.960ms</td></tr>
<tr><td>1101</td><td>81.920ms</td></tr>
<tr><td>1110</td><td>163.840ms</td></tr>
<tr><td>1111</td><td>327.680ms</td></tr>
</table>
</td><td>R/W</td><td>1000</td></tr>
</table>

Table 5-12: Auto Status Timer Register (Offset 0x94)

5.3 DAC Data Space

PCI Base Address: PCI9030 PCI Base Address 3 (Offset 0x1C in PCI Configuration Space).

The DAC Data Space provides a 16 bit address location for each of the D/A channels and is used for passing D/A Channel data in I-Mode, M-Mode and T-Mode. 16 bit or 32 bit transfer sizes may be used.

D/A Channels 1 to 4 belong to Q-DAC 1, D/A Channels 5 to 8 belong to Q-DAC 2, and so on.

For I-Mode or M-Mode: If data is written to the DAC data space, the data is transferred to the appropriate Q-DAC (via the Q-DAC serial interface) as soon as possible. Data may be written to the DAC data space while a Q-DAC data transfer is in progress. E.g. data for D/A channels 3 & 4 may be written to the DAC data space while the data for D/A channel 1 is actually being transferred to the Q-DAC and thus the Q-DAC Busy Bit is set in the Global Status Register.

16 bit or 32 bit transfer size must be used for accessing the DAC Data Space.

To optimize data throughput, this space allows 32 bit accesses, which target two subsequent 16 bit words (D/A Channels) (note that the TPMC553 local spaces are set to Big Endian mode).

The DAC data space is readable, but the read values are just showing the value of the previous write to the DAC data space location (they are not read-back from the Q-DAC internal data registers).

Offset to PCI Base Address 3	Description	Q-DAC	Q-DAC internal Channel	Size (Bit)
0x00	D/A Channel 1 Data	Q-DAC 1	A	16
0x02	D/A Channel 2 Data		B	16
0x04	D/A Channel 3 Data		C	16
0x06	D/A Channel 4 Data		D	16
0x08	D/A Channel 5 Data	Q-DAC 2	A	16
0x0A	D/A Channel 6 Data		B	16
0x0C	D/A Channel 7 Data		C	16
0x0E	D/A Channel 8 Data		D	16
0x10	D/A Channel 9 Data	Q-DAC 3	A	16
0x12	D/A Channel 10 Data		B	16
0x14	D/A Channel 11 Data		C	16
0x16	D/A Channel 12 Data		D	16
0x18	D/A Channel 13 Data	Q-DAC 4	A	16
0x1A	D/A Channel 14 Data		B	16
0x1C	D/A Channel 15 Data		C	16
0x1E	D/A Channel 16 Data		D	16

Offset to PCI Base Address 3	Description	Q-DAC	Q-DAC internal Channel	Size (Bit)
0x20	D/A Channel 17 Data	Q-DAC 5	A	16
0x22	D/A Channel 18 Data		B	16
0x24	D/A Channel 19 Data		C	16
0x26	D/A Channel 20 Data		D	16
0x28	D/A Channel 21 Data	Q-DAC 6	A	16
0x2A	D/A Channel 22 Data		B	16
0x2C	D/A Channel 23 Data		C	16
0x2E	D/A Channel 24 Data		D	16
0x30	D/A Channel 25 Data	Q-DAC 7	A	16
0x32	D/A Channel 26 Data		B	16
0x34	D/A Channel 27 Data		C	16
0x36	D/A Channel 28 Data		D	16
0x38	D/A Channel 29 Data	Q-DAC 8	A	16
0x3A	D/A Channel 30 Data		B	16
0x3C	D/A Channel 31 Data		C	16
0x3E	D/A Channel 32 Data		D	16

Table 5-13: DAC Data Space Address Map

5.4 DAC Calibration Data Space

PCI Base Address: PCI9030 PCI Base Address 4 (Offset 0x20 in PCI Configuration Space).

The calibration data values are determined at factory and are stored in this read-only space.

There is an Offset Correction value and a Gain Correction value for each D/A Channel at each voltage range.

16 bit or 32 bit transfer size must be used for accessing the Calibration Data Space.

See the Programming Hints chapter for data correction formulas.

The calibration data is loaded from a serial EEPROM after power-up or PCI reset and is available approx. 8 ms after PCI reset.

The correction factors are stored consecutive in 16 bit values, in order of the D/A Channels 1-32, starting with D/A Channel 1.

Offset to PCI Base Address 5	Description	D/A Channel	Voltage Range
0x000	$Offset_{corr}$	1	0V … +5V
0x002	$Offset_{corr}$	2	0V … +5V
…	…	…	…
0x03E	$Offset_{corr}$	32	0V … +5V
0x040	$Gain_{corr}$	1	0V … +5V
0x042	$Gain_{corr}$	2	0V … +5V
…	…	…	…
0x07E	$Gain_{corr}$	32	0V … +5V
0x080	$Offset_{corr}$	1	0V … +10V
0x082	$Offset_{corr}$	2	0V … +10V
…	…	…	…
0x0BE	$Offset_{corr}$	32	0V … +10V
0x0C0	$Gain_{corr}$	1	0V … +10V
0x0C2	$Gain_{corr}$	2	0V … +10V
…	…	…	…
0x0FE	$Gain_{corr}$	32	0V … +10V
0x100	$Offset_{corr}$	1	0V … +10.8V
0x102	$Offset_{corr}$	2	0V … +10.8V
…	…	…	…
0x13E	$Offset_{corr}$	32	0V … +10.8V
0x140	$Gain_{corr}$	1	0V … +10.8V
0x142	$Gain_{corr}$	2	0V … +10.8V
…	…	…	…

Offset to PCI Base Address 5	Description	D/A Channel	Voltage Range
0x17E	$Gain_{corr}$	32	0V … +10.8V
0x180	$Offset_{corr}$	1	±5V
0x182	$Offset_{corr}$	2	±5V
…	…	…	…
0x1BE	$Offset_{corr}$	32	±5V
0x1C0	$Gain_{corr}$	1	±5V
0x1C2	$Gain_{corr}$	2	±5V
…	…	…	…
0x1FE	$Gain_{corr}$	32	±5V
0x200	$Offset_{corr}$	1	±10V
0x202	$Offset_{corr}$	2	±10V
…	…	…	…
0x23E	$Offset_{corr}$	32	±10V
0x240	$Gain_{corr}$	1	±10V
0x242	$Gain_{corr}$	2	±10V
…	…	…	…
0x27E	$Gain_{corr}$	32	±10V
0x280	$Offset_{corr}$	1	±10.8V
0x282	$Offset_{corr}$	2	±10.8V
…	…	…	…
0x2BE	$Offset_{corr}$	32	±10.8V
0x2C0	$Gain_{corr}$	1	±10.8V
0x2C2	$Gain_{corr}$	2	±10.8V
…	…	…	…
0x2FE	$Gain_{corr}$	32	±10.8V

Table 5-14: DAC Calibration Data Space Address Map

6 Functional Description

6.1 Q-DAC Configuration

Each Q-DAC must be configured before usage, right after power-up or reset. See the Q-DAC Configuration Register for Q-DAC configuration options.

A Q-DAC is being configured by a write to the appropriate Q-DAC Configuration Register (there is a Q-DAC Configuration Register for each Q-DAC) while the Q-DAC Busy bit in the Global Status Register is clear. Writes to a Q-DAC Configuration Registers are ignored when the Q-DAC Busy bit is set for this Q-DAC.

When the Q-DAC configuration is started, the Q-DAC Busy bit in the Global Status Register is set and the Q-DAC configuration is transferred to the Q-DAC internal configuration registers via the Q-DAC serial interface.

Check the Q-DAC Busy bits in the Global Status Register to determine when a certain Q-DAC configuration is done.

Steps for Q-DAC configuration:

- Check the Q-DAC Busy bit(s) is (are) clear in the Global Status Register
- Write the Q-DAC configuration setup to the Q-DAC Configuration Register(s)
- Wait until the Q-DAC Busy bit(s) is (are) clear in the Global Status Register
- Check the Q-DAC Status Register(s) (e.g. check that all Q-DAC internal DACs are powered-up, etc.)

6.2 Q-DAC Modes

Each Q-DAC (i.e. a group of four D/A channels) can be set to I-Mode, M-Mode or T-Mode operation. The Q-DAC mode is set in the Q-DAC Control Register.

The Q-DAC mode should be setup soon after Q-DAC configuration and before any other Q-DAC action than Q-DAC configuration.

The Q-DAC Busy bit in the Global Status Register shall be checked to be clear before the Q-DAC mode is altered from the default I-Mode.

6.2.1 I-Mode (Instant Mode)

6.2.1.1 Setting I-Mode

(it is assumed that the Q-DACs are already configured)

Instant Mode is the default Q-DAC mode after power-up or reset.

The following steps may be used if it is desired to set a Q-DAC back to I-Mode:

- Check the Q-DAC Busy bit is clear in the Global Status Register
- Set the Q-DAC Mode to I-Mode in the Q-DAC Control Register

6.2.1.2 Using I-Mode

Data written to the DAC data space is transferred to the appropriate Q-DAC as soon as possible. The D/A channel analog output is automatically updated when the data has actually been transferred to the Q-DAC.

Each Q-DAC covers four D/A channels and provides a single serial interface.

If any D/A channel data is updated at a rate higher than 100kHz, data may get lost (depends on what and how many D/A channels are used and whether the Q-DAC status is read; less than four D/A channels per Q-DAC without Q-DAC status read may be updated at a higher rate). The settling of an analog output takes up to 10us (100kHz).

Max D/A channel data update rate without data loss (without Q-DAC status read):

1 / (*number_of_qdac_dacs_used* x 1.4us) *number_of_qdac_dacs_used* = 1 to 4

Max. D/A channel data update rate without data loss (with Q-DAC status read):

1 / ((*number_of_qdac_dacs_used* x 1.4us) + 3.4us) *number_of_qdac_dacs_used* = 1 to 4

Note, that for fastest D/A channel analog output update rate the used D/A channels should be spread over the various Q-DACs. E.g. when using D/A channels 1, 2, 3 & 4 the D/A channel data must be transferred to Q-DAC 1 one after the other and so the max D/A channel data update rate is 178kHz. When using D/A channels 1, 5, 9 & 13, the data is transferred to the Q-DACs 1, 2, 3 & 4 at the same time and so the max D/A channel data update rate is 714 kHz. Note also that the analog output settling time for each D/A channel is 10us max (100 kHz).

Software may wait to see the Q-DAC busy bit clear in the Global Status Register before new data is written for a Q-DAC. Up to four D/A channels per Q-DAC could be updated then, using two 32 bit or four 16 bit writes to the appropriate DAC data space locations.

There are no options for a simultaneous load (analog output update) between D/A channels or Q-DACs in this mode. Each D/A channel analog output is updated individually if the D/A channel data has been transferred to the Q-DAC.

6.2.2 M-Mode (Manual Mode)

6.2.2.1 Setting M-Mode

(it is assumed that the Q-DACs are already configured)

The following steps should be used to set a Q-DAC to M-Mode:

- Check the Q-DAC Busy bit is clear in the Global Status Register
- Set the Q-DAC Mode to M-Mode in the Q-DAC Control Register (along with the Global Mode bit if desired)

6.2.2.2 Using M-Mode

Data written to the DAC data space is transferred to the appropriate Q-DAC as soon as possible, but the Q-DAC analog outputs are not automatically updated when the data transfer is done.

Setting the Load bit in the Load Register logs a request for updating the Q-DAC analog outputs.

In **Standalone M-Mode**, the update of the Q-DAC analog outputs is delayed until all available D/A channel data has been transferred to the Q-DAC. The four D/A channel analog outputs of the Q-DAC are updated simultaneously.

In **Global M-Mode**, the update of the Q-DAC analog outputs is delayed until all available D/A channel data has been transferred to all the Q-DACs that are set to Global M-Mode. The D/A channel analog outputs of all Q-DACs in Global M-Mode are updated simultaneously.

See the Global Load Mode bit in the Q-DAC Control Register description.

Method A (the load command is set during the data transfer)**:**

- Check the Q-DAC Load bit is clear in the Load Register
- Write new D/A channel data to the DAC data space (i.e. transfer new data to the Q-DAC)
- Set the Q-DAC Load bit in the Load Register (the Q-DAC load is delayed until all available data has been transferred to the Q-DAC)
- Wait until the Q-DAC Load bit is clear in the Load Register (i.e. wait until the Q-DAC analog outputs have been updated)
- Write new D/A channel data to the DAC data space (i.e. transfer new data to the Q-DAC)
- and so on

Method B (data is transferred completely before the load command is set)**:**

- Check the Q-DAC Busy bit is clear in the Global Status Register
- Write Q-DAC data to the DAC data space (i.e. transfer new data to the Q-DAC)
- Wait until the Q-DAC Busy bit is clear in the Global Status Register (i.e. wait until all data has been transferred to the Q-DAC)
- Set the Q-DAC Load bit in the Load Register (quick Q-DAC load response, since the data has already been transferred to the Q-DAC before)
- Wait until the Q-DAC Busy bit is clear in the Global Status Register (i.e. wait until the Q-DAC analog outputs have been updated)
- Write Q-DAC data to the DAC data space (i.e. transfer new data to the Q-DAC)
- and so on

6.2.3 T-Mode (Timer / Sequencer Mode)

6.2.3.1 Preparing for T-Mode

(it is assumed that the Q-DACs are already configured)

- Set the Q-DAC Sequencer Timer Register
- Check the Q-DAC Busy bit is clear in the Global Status Register
- Set the Q-DAC Mode to T-Mode in the Q-DAC Control Register
- For interrupt controlled sequencer serving only: enable Q-DAC sequencer interrupt in the Q-DAC Control Register
- Write the Q-DAC data for the first sequence to the DAC Data Space

6.2.3.2 Starting the Sequencer

If preparing for Timer / Sequencer Mode is completed, the Sequencer for a Q-DAC is started by setting the Sequencer Start/Stop bit in the Global Control Register.

For a simultaneous D/A channel update between Q-DACs, the Q-DAC timers must be set to the same value and the Q-DAC sequencers must be started simultaneously with the same write access to the Global Control Register.

6.2.3.3 Serving the Sequencer

6.2.3.3.1 Polling Mode

- Poll the Q-DAC Sequencer Data Request bit in the Global Status Register until the bit is set
- The Q-DAC Sequencer Underflow bit in the Global Status Register may be checked then
- Write new Q-DAC data to the DAC data space
- Clear the Q-DAC Sequencer Data Request bit in the Global Status Register
- Poll the Q-DAC Sequencer Data Request bit in the Global Status Register until the bit is set
- and so on

6.2.3.3.2 Interrupt Mode

Upon Interrupt: Check the Interrupt Status Register for Q-DAC sequencer interrupt.

Upon Sequencer Interrupt:

- Check the Q-DAC Sequencer Data Request bit and the Q-DAC Sequencer Underflow bit in the Global Status Register
- Write the Q-DAC data for the next sequence to the appropriate location in the DAC data space (if the data for a D/A channel has not changed, it does not need to be written again).
- Clear the Q-DAC Sequencer Data Request bit in the Global Status Register
- Clear the Q-DAC Sequencer Interrupt Status bit in the Interrupt Status Register

6.2.3.4 Stopping the Sequencer

The Sequencer is stopped by clearing the Sequencer Start / Stop bit in the Global Control Register.

Any ongoing data transfer to the Q-DAC will continue and terminate normally. Check the Q-DAC Busy bit in the Global Status Register to determine when the Sequencer is actually stopped.

6.3 Q-DAC Status

The Q-DAC device used provides an internal status register that could be read from the Q-DAC. See the Q-DAC Status Register for details.

6.3.1 Manual Status Read

Manual Q-DAC status read is supported for I-Mode and M-Mode (not supported for T-Mode).

In I-Mode and M-Mode, setting the Read Status Register bit in the Q-DAC Control Register logs a request for reading the status of the Q-DAC device.

When the status read request is logged, the Status Valid bit in the Q-DAC Status Register is cleared. The Status Valid bit in the Q-DAC Status Register is automatically set again when the Q-DAC status read is done and the Q-DAC Status Register has been updated.

If there is any Q-DAC data transfer in progress, the Q-DAC status read is delayed until the current Q-DAC data transfer is done. If the Q-DAC is actually waiting for a global simultaneous load in Global M-Mode, the Q-DAC status read is delayed until the global simultaneous load is done.

6.3.2 Automatic Status Read

Automatic Q-DAC status read is supported for I-Mode, M-Mode and T-Mode.

Automatic Q-DAC status read is enabled in the Q-DAC Control Register.

In I-Mode and M-Mode, a request for reading the Q-DAC status is logged every time the Q-DAC Auto Status Timer expires (cyclic timer). See the Auto Status Timer Register for details.

If there is any Q-DAC data transfer in progress, the Q-DAC status read is delayed until the current Q-DAC data transfer is done. If the Q-DAC is actually waiting for a global simultaneous load in Global M-Mode, the Q-DAC status read is delayed until the global simultaneous load is done.

In T-Mode, there is one Q-DAC status update per sequence.

7 Programming Hints

7.1 DAC Output Coding

Analog Output	Bipolar Output, Twos Complement Coding			Digital Input
Output Range	±5V	±10V	±10.8V	
Least Significant Bit	152.59µV	305.18µV	329.59µV	
+FSR	4.999847V	9.999695V	10.79967V	0x7FFF
+FSR - 1LSB	4.999695V	9.99939V	10.79934V	0x7FFE
Midscale + 1LSB	152.59µV	305.18µV	329.59µV	0x0001
Midscale	0V	0V	0V	0x0000
Midscale - 1LSB	-152.59µV	-305.18µV	-329.59µV	0xFFFF
-FSR + 1LSB	-4.999847V	-9.999695V	-10.79967V	0x8001
-FSR	-5	-10V	-10.8V	0x8000

Table 7-1 : DAC Output Coding, Bipolar Output Range

Analog Output	Unipolar Output, Straight Binary Coding			Digital Input
Output Range	+5V	+10V	+10.8V	
Least Significant Bit	76.29µV	152.59µV	164.79µV	
FSR	4.999924V	9.999847V	10.799835V	0xFFFF
FSR - 1LSB	4.999847V	9.999695V	10.79967V	0xFFFE
Midscale + 1LSB	2.500076V	5.000153V	5.400165V	0x8001
Midscale	2.5V	5V	5.4V	0x8000
Midscale - 1LSB	2.499924V	4.999847V	5.399835V	0x7FFF
0V + 1LSB	76.29µV	152.59µV	164.79µV	0x0001
0V	0V	0V	0V	0x0000

Table 7-2 : DAC Output Coding, Unipolar Output Range

7.2 DAC Data Correction

There are two errors which affect the DC accuracy the DACs.

- Offset Error: The data value that is required to get a zero voltage output signal. This error is corrected by subtracting the known error from the data value.
- Gain Error: The difference between the ideal gain and the actual gain of the DAC. It is corrected by multiplying the data value with a correction factor.

The data correction values are obtained during factory calibration and are stored in the Calibration Data Space.

7.2.1 DAC Correction Values

The data correction values are obtained during factory calibration and are stored in the Calibration Data Space.

The corrections values are obtained the following way:

- First the DAC D/A function is determined by measuring the analog output voltage at several bit values at a given operating temperature.
- Then a regression line is calculated that fits best into the determined DAC D/A function (which in general is a curve with offset and gain errors).
- Both *Offset_Error* and *Gain_Error* are taken from the calculated regression line of the D/A function (*Offset_Error* is the A value at D = 0, *Gain_Error* is the deviation of the A value from the ideal A value at D = Full Scale).
- The *Offset_Corr* (= *Offset_Error* x 4) and *Gain_Corr* (= *Gain_Error* x 4) values are stored in a serial EEPROM. These values could be read in the Calibration Data Space.
- *Offset_Corr* and *Gain_Corr* values are available for every DAC channel and every output voltage range.

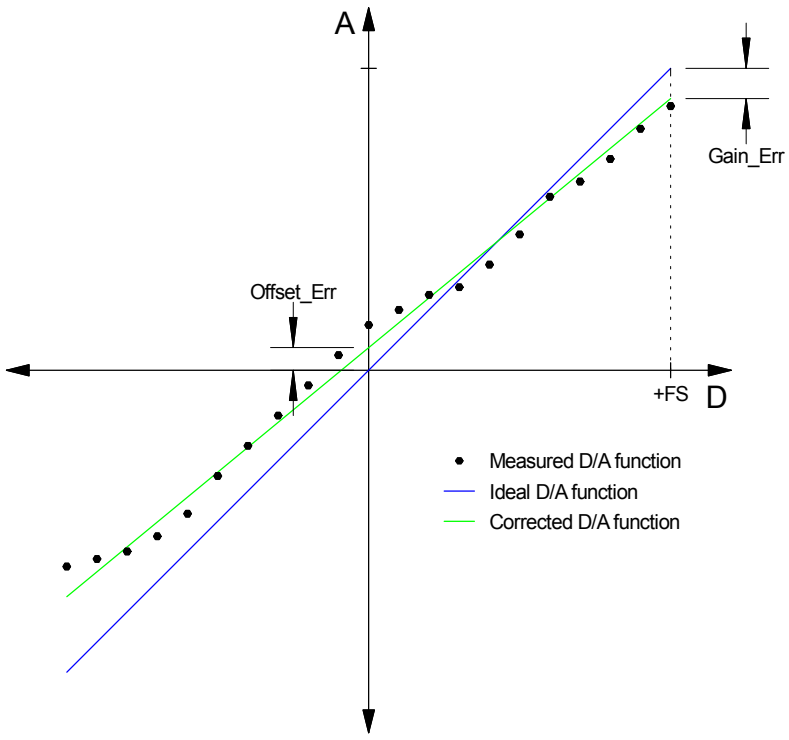

Figure 7-1: Principle of DAC D/A correction

7.2.2 DAC Correction Formula

7.2.2.1 Unipolar Output Voltage Ranges

The basic formula for correcting the DAC value is:

$$Data = Value \cdot \left(1 - \frac{Gain_{corr}}{262144}\right) - \frac{Offset_{corr}}{4}$$

Value is the desired DAC value.

Data is the corrected DAC value that must be sent to the DAC.

$Gain_{corr}$ and $Offset_{corr}$ are the DAC correction values from the Calibration Data Space. They are stored separately for each of the 32 DAC channels and each output voltage range mode.

The correction values are stored as two's complement 16 bit wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

7.2.2.2 Bipolar Output Voltage Ranges

The basic formula for correcting the DAC value is:

$$Data = Value \cdot \left(1 - \frac{Gain_{corr}}{131072}\right) - \frac{Offset_{corr}}{4}$$

Value is the desired DAC value.

Data is the corrected DAC value that must be sent to the DAC.

$Gain_{corr}$ and $Offset_{corr}$ are the DAC correction values from the Calibration Data Space. They are stored separately for each of the 32 DAC channels and each output voltage range mode.

The correction values are stored as two's complement 16 bit wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic must be used to avoid rounding errors in computing above formula.

Due to inherent DAC device deviation, the extremes of the full scale range may not be fully reachable, even after calibration.

8 Pin Assignment – I/O Connector

8.1 Front I/O Connector

Pin-Count	68
Connector Type	HD68 / SCSI-3
Source & Order Info	AMP 5-787082-7 or compatible

Table 8-1 : I/O Front Connector Type

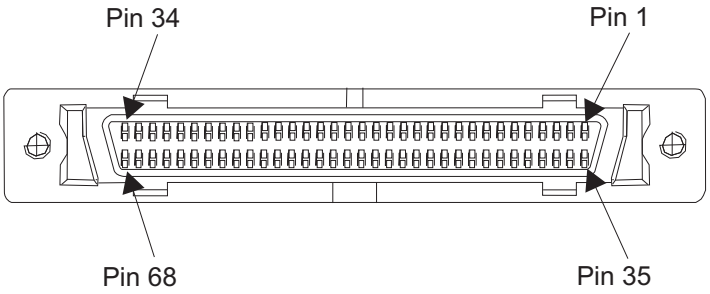

Figure 8-1: I/O Front Connector View

8.2 Pin Assignment

Each D/A channel should share a twisted cable pair with GND.

Pin	Signal
1	D/A Channel 1
2	D/A Channel 2
3	D/A Channel 3
4	D/A Channel 4
5	D/A Channel 5
6	D/A Channel 6
7	D/A Channel 7
8	D/A Channel 8
9	D/A Channel 9
10	D/A Channel 10
11	D/A Channel 11
12	D/A Channel 12
13	D/A Channel 13
14	D/A Channel 14
15	D/A Channel 15
16	D/A Channel 16
17	D/A Channel 17
18	D/A Channel 18

Pin	Signal
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	GND
49	GND
50	GND
51	GND
52	GND

Pin	Signal	Pin	Signal
19	D/A Channel 19	53	GND
20	D/A Channel 20	54	GND
21	D/A Channel 21	55	GND
22	D/A Channel 22	56	GND
23	D/A Channel 23	57	GND
24	D/A Channel 24	58	GND
25	D/A Channel 25	59	GND
26	D/A Channel 26	60	GND
27	D/A Channel 27	61	GND
28	D/A Channel 28	62	GND
29	D/A Channel 29	63	GND
30	D/A Channel 30	64	GND
31	D/A Channel 31	65	GND
32	D/A Channel 32	66	GND
33	NC	67	GND
34	NC	68	GND

Table 8-2 : I/O Pin Assignment