The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC815

ARCNET PMC

Version 2.0

User Manual

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TPMC815-11

ARCNET PMC

Traditional Hybrid Interface (2.5 Mbps)

TPMC815-21

ARCNET PMC

Isolated RS485 Interface (5 Mbps)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Initial Issue	January 2001
1.1	Corrections in PCI Target Chip Section	May 2002
1.2	Module Version Change (PCI Target Chip)	November 2002
1.3	New address TEWS LLC	September 2006
1.4	Hybrid Vendor has changed Hybrid Circuit Parameters as part of the RoHS transition. The TPMC815-11 no longer supports 5 Mbps.	January 2007

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1 Product Description

The TPMC815 provides a complete ARCNET interface using the COM20020 ARCNET controller from SMSC. The TPMC815 is ideal suited for industrial / factory automation and automotive applications. Various network topologies are supported (Star, Tree, and Bus).

The COM20020 additionally provides 2 K x 8 bit dual port RAM.

The following TPMC815 options are available:

The **TPMC815-11 (max 2.5 Mbps)** provides the **traditional isolated hybrid interface** available on either the BNC connector or the DB9 connector (selected by jumper).

The **TPMC815-21 (max 5 Mbps)** provides an **isolated RS485 differential driver interface** available on the DB9 connector.

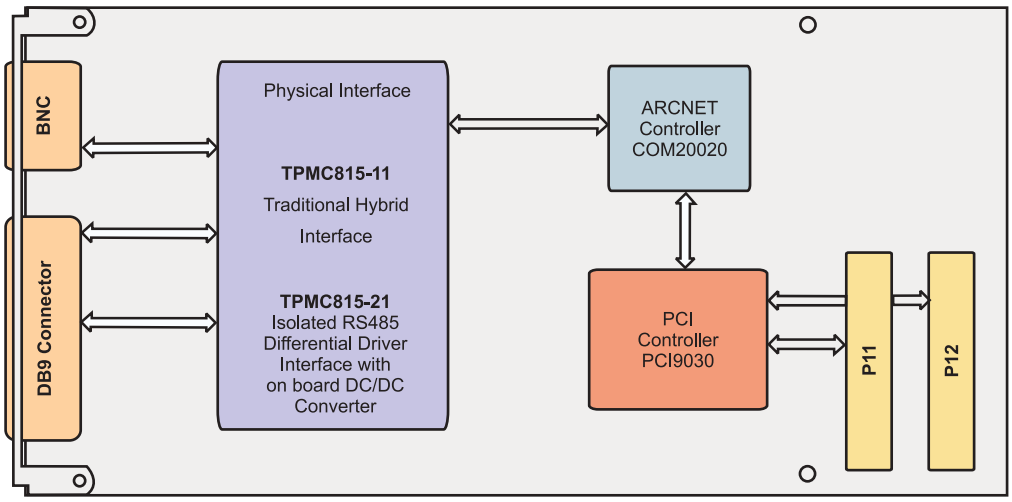

Figure 1-1 : Block Diagram

2 Technical Specification

Logic Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 3.3V PCI Signaling Voltage. 5V PCI Signaling Voltage tolerant.	
On Board Devices		
PCI Target Chip	PCI9030 (PLX Technology)	
Arcnet Controller	COM20020 (SMSC)	
I/O Interface		
Physical Interface	TPMC815-11: Isolated Hybrid (Coax 90ohms or Twisted Pair) TPMC815-21: Isolated RS485	
Transfer Rates	TPMC815-11: 2.5 Mbps, 1.25 Mbps or 625 Kbps TPMC815-21: 5 Mbps, 2.5 Mbps, 1.25 Mbps or 625 Kbps software selectable	
I/O Interface	TPMC815-11: DB9 male connector, BNC 90ohms TPMC815-21: DB9 male connector	
Physical Data		
Power Requirements	TPMC815-11	250mA max. @ +3.3V 600mA max. @ +5V 0.15A max. @ -12V +12V Not Used
	TPMC815-21	250mA max. @ +3.3V 300mA max. @ +5V +12V, -12V Not Used
Temperature Range	TPMC815-11	Operating : 0°C to +70°C Storage : –55°C to +150°C
	TPMC815-21	Operating : -40°C to +85°C Storage : –55°C to +150°C
MTBF	TPMC815-11	351000 h
	TPMC815-21	312000 h
Weight	72 g	
Humidity	5 – 95 % non-condensing	

Figure 2-1 : Technical Specification

3 Functional Description

The TPMC815 uses the COM20020 ARCNET Controller from SMSC.

The COM20020 registers are accessible in PCI Space using the local spaces of the PCI9030 PCI Target Chip.

The complete TPMC815 ARCNET interface is controlled by the COM20020 ARCNET Controller.

Please refer to the COM20020 data sheet for a detailed functional description.

The TPMC815 also provides an 8 x dip-switch. Software may use the dip-switch setting for programming the COM20020 Node-ID Register.

4 Local Space Addressing

4.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	IO	16	8	LIT	Local Register Space
1	3 (0x1C)	MEM	256	8	LIT	Local Register Space
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Figure 4-1 : PCI9030 Local Space Configuration

4.2 Local Register Space Address Map

PCI Base Address =

PCI I/O Space Mapped:
PCI9030 PCI Base Address 2 (Offset 0x18 in PCI9030 PCI Configuration Space)

PCI MEM Space Mapped:
PCI9030 PCI Base Address 3 (Offset 0x1C in PCI9030 PCI Configuration Space)

Offset to PCI Base Address	Register Name	Size (Bit)
COM20020 Registers		
0x00	Status / Interrupt Mask	8
0x01	Diagnostic Status / Command	8
0x02	Address Pointer High	8
0x03	Address Pointer Low	8
0x04	Data	8
0x05	Sub Address	8
0x06	Configuration	8
0x07	Tentative ID	8
	Node ID	
	Setup 1	
	Next ID / Test	
	Setup 2	
Additional Registers		
0x08	ID Switch	8

Figure 4-2 : Local Register Space

4.2.1 COM20020 Registers

Please refer to the COM20020 datasheet for a detailed description of the COM20020 ARCNET Controller registers.

4.2.2 ID Switch Register

The ID Switch Register is an 8 bit read only register representing the actual setting of the on board 8 x dip-switches.

Bit	Switch No.	Access	Bit Value
7 (msb)	8	R	Switch Position ON = Bit value '0' Switch Position OFF = Bit value '1'
6	7		
5	6		
4	5		
3	4		
2	3		
1	2		
0 (lsb)	1		

Figure 4-3 : ID Switch Register

Software may read the ID Switch Register to program the COM20020 Node-ID Register.

5 PCI9030 Target Chip

5.1 PCI Configuration Registers (PCR)

5.1.1 PCI9030 PCI Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	032F 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	028000 00
0x0C	BIST	Header Type	Latency Timer	Cacheline Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFFF1
0x1C	PCI Base Address 3 for Local Address Space 1				Y	FFFFFF00
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	s.b. 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt. Cap.	PM Cap. ID	N	4801 48 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt. Cap.	HS Cap. ID	Y[23:16]	00 00 4C 06
0x4C	VPD Address		VPD Nxt. Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Figure 5-1 : PCI9030 PCI Header

Subsystem-ID: TPMC815-11: 0x000B

TPMC815-21: 0x0015

5.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9030 PCI Base Address Initialization:

1. Write 0xFFFF_FFFF to the PCI9030 PCI Base Address Register.
2. Read back the PCI9030 PCI Base Address Register.
3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space:

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage:

   Bit 0 = ‘0’: Expansion ROM not used

   Bit 0 = ‘1’: Expansion ROM used
4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to ‘1’, the PCI9030 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).
5. Determine the base address and write the base address to the PCI9030 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9030 PCI Base Address Register.

After programming the PCI9030 PCI Base Address Registers, software must enable the PCI9030 for PCI I/O and/or PCI Memory Space access in the PCI9030 PCI Command Register (Offset 0x04):

To enable PCI I/O Space access to the PCI9030, set bit 0 to '1'.

To enable PCI Memory Space access to the PCI9030, set bit 1 to '1'.

5.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is:

PCI9030 PCI Base Address 0 (PCI Memory Space mapped) (Offset 0x10 in the PCI Configuration Register Space)

PCI9030 PCI Base Address 1 (PCI I/O Space mapped) (Offset 0x14 in the PCI Configuration Register Space)

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FFF1
0x04	Local Address Space 1 Range	0x0FFF_FF00
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Local Exp. ROM Range	0x0000_0000
0x14	Local Address Space 0 Remap	0x0000_0001
0x18	Local Address Space 1 Remap	0x0000_0001
0x1C	Local Address Space 2 Remap	0x0000_0000
0x20	Local Address Space 3 Remap	0x0000_0000
0x24	Local Exp. ROM Remap	0x0000_0000
0x28	Local Address Space 0 Descriptor	0x5401_E0E0
0x2C	Local Address Space 1 Descriptor	0x5401_E0E0
0x30	Local Address Space 2 Descriptor	0x0000_0000
0x34	Local Address Space 3 Descriptor	0x0000_0000
0x38	Local Exp. ROM Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0004
0x40	Chip Select 1 Base Address	0x0000_000C
0x44	Chip Select 2 Base Address	0x0000_0000
0x48	Chip Select 3 Base Address	0x0000_0000
0x4C	Interrupt Control/Status	0x0041
0x4E	EEPROM Write Protect Boundary	0x0030
0x50	Miscellaneous Control Register	0x0078_0000
0x54	General Purpose I/O Control	0x0224_9249
0x70	Hidden1 Power Management	0x0000_0000
0x74	Hidden 2 Power Management	0x0000_0000

Figure 5-2 : PCI9030 Local Configuration Register

5.3 Configuration EEPROM

After power-on or PCI reset the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x032F	0x1498	0x0280	0x0000	0x0280	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFFF1	0x0FFF	0xFF00
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0001	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x5401	0xE0E0	0x5401	0xE0E0	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0004	0x0000	0x000C	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x0000	0x0224	0x9249
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Figure 5-3 : Configuration EEPROM TPMC815

Subsystem-ID Value (EEPROM Offset 0x0C): TPMC815-11: 0x000B

TPMC815-21: 0x0015

5.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of 1 resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers and the PCI9030 PCI Interface are not reset.

6 Programming Notes

6.1 COM20020 Controller

6.1.1 Hardware Initialization

The COM20020 ARCNET Controller, which is used on the TPMC815, is able to work with different CPU bus structures. The COM20020 device learns the used bus structure by monitoring the first bus cycles which address the COM20020.

To initialize the COM20020 ARNET Controller to the right CPU bus structure the software must do the following accesses to the COM20020 immediately after a system reset:

1. **Write 0x55 to the Command Register at byte offset 0x01.**
2. **Read the Diagnostic Status Register at byte offset 0x01.**

If after a reset, the COM20020 is not initialized with the sequence listed above, the ARCNET PMC will not operate properly.

6.1.2 Clock Source

On the TPMC815 the COM20020 ARCNET Controller is sourced with a 40 MHz clock.

6.1.3 Programming

For programming the COM20020 ARCNET Controller please refer to the COM20020 data sheet.

7 Installation Notes

7.1 On board ID Switch

The TPMC815 provides an on board 8 x dip-switches. The switch setting can be read by software at initialization time where the value may be used to program the node ID of the COM20020 ARCNET Controller.

A switch in position OFF represents a logical ‘1’, a switch in position ON represents a logical ‘0’.

Factory configuration: All dip-switches are set in OFF position (representing the byte value 0xFF).

7.2 Wiring Hints / Network Cabling

7.2.1 Coax

RG62 is the most popular ARCNET cable. Other cable types may be used, but RG62 offers the best electrical characteristics as well as a low cost. It is first choice for even difficult, electrically noisy environments. It is also simple to install and terminate.

7.2.2 Twisted Pair and RS485

For a Twisted Pair or RS485 network a twisted pair cable with an impedance of 100ohms @ 1 MHz should be used. It can be AWG 22, 24, 26.

All network signal lines must be terminated at both extremes of the cabling network with a resistor connected between Phase A and Phase B for Twisted Pair, or between Signal + and Signal – for RS485. The resistor value should be equal to the impedance of the cable.

RS485 Notes (TPMC815-21 only):

The TPMC815-21 provides on board RS485 line termination which can be enabled or disabled by jumpers.

The on board RS485 line termination is:

120R between the isolated RS484 Signals, 1K5 between isolated RS485 Signal + and isolated RS485 supply (+5V), 1K5 between isolated RS485 Signal – and isolated RS485 GND.

If the bus is build with TPMC815 modules only, the two TPMC815 modules at the bus ends must have the termination jumpers enabled, while the other TPMC815 modules must have the termination jumpers disabled.

If a TPMC815 module is used together with other modules that provide fixed on board bias termination, the TPMC815 termination jumpers should be disabled. In this case, if a TPMC815 module should be placed at a bus end, use external bus termination.

7.3 Jumper Configuration

The TPMC815-11 is configured by the jumpers J1 and J2.

J1 sets the termination mode for the coax interface.
J2 selects the desired network media: coax or twisted pair.

The TPMC815-21 is configured by the jumpers J3 and J4.

J3 and J4 set the on board RS485 line termination mode.

Jumper	Function	Installation	Option
		TPMC815-11	
J1	Coax Termination Mode	Closed	Coax Termination ON (93ohms)
		Open	Coax Termination OFF
J2	Media Selection	1-3, 2-4	Coax Cable (BNC)
		3-5, 4-6	Twisted Pair Cable (DB9)
		TPMC815-21	
J3, J4	RS485 Termination Mode	Both Closed	RS485 Line Termination ON
		Both Open	RS485 Line Termination OFF

Figure 7-1 : Jumper Configuration

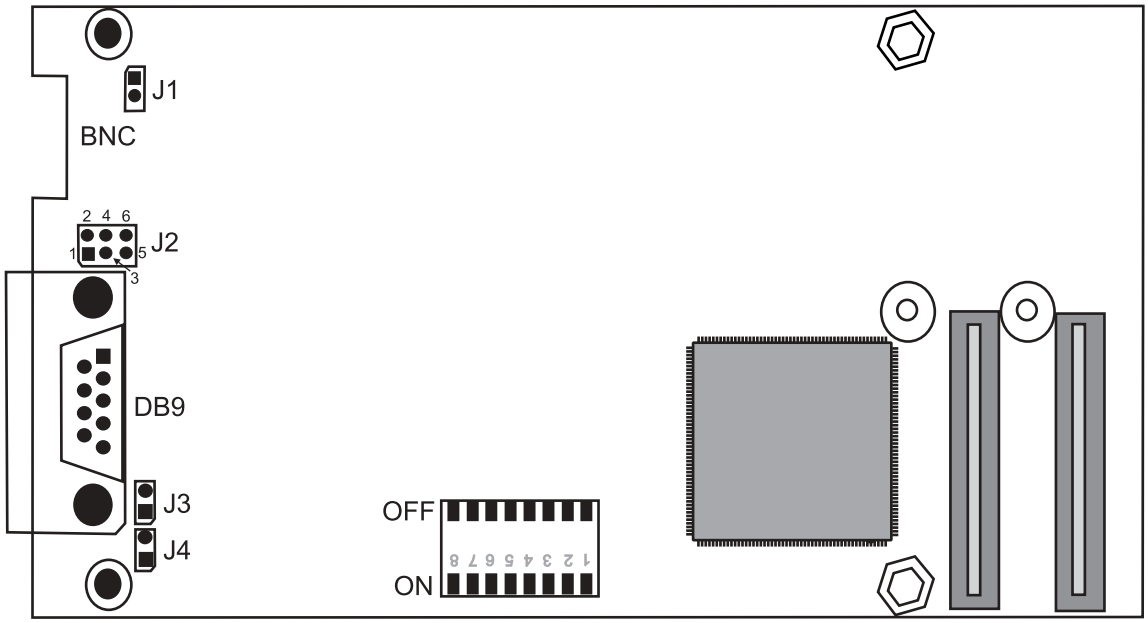

Figure 7-2 : Jumper Location

8 Pin Assignment – I/O Connector

8.1 DB9 Front I/O Connector

Pin	Signal	Comment
1	Isolated RS485 Signal 2	TPMC815-21 Only
2	Isolated RS485 Signal 1	TPMC815-21 Only
3	N.C.	
4	Twisted Pair Phase B	TPMC815-11 Only
5	Twisted Pair Phase A	TPMC815-11 Only
6	Isolated GND	
7	Isolated GND	
8	N.C.	
9	Isolated GND	

Figure 8-1 : Pin Assignment I/O Connector