The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC884

Dual Channel 10/100/1000 Mbit/s Ethernet Adapter

Version 1.0

User Manual

Issue 1.0.4

July 2009

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TPMC884-10

Dual Channel 10/100/1000 Mbit/s Ethernet Adapter
Front panel connector
Based on Intel 82546EB Ethernet Controller

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	August 2004
1.1	EPROM Data correction	June 2005
1.2	New address TEWS LLC	September 2006
1.3	RoHS compliant version added	March 2008
1.0.4	New User Manual Issue Notation Documentation of RoHS compliant and non-RoHS compliant Version is now in separate documents	July 2009

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1 Product Description

The TPMC884 is a PCI Mezzanine Card (PMC) compatible module providing a dual channel Gigabit Ethernet 10 / 100 / 1000BASE-TX interface.

For highest data rates, the TPMC884 has a 64 bit, 133/100/66 MHz PCI bus interface and is capable of full speed bus-master DMA operations utilizing maximum PCI bandwidth.

An Intel™ 82546EB Ethernet Controller is used, which supports 10, 100 and 1000 Mbit/s transmission rates for half and full duplex operation. The TPMC884 is capable of performing an auto negotiation algorithm which allows both link-partners to find out the best link-parameters by themselves. The TPMC884 is widely user configurable via configuration and status register access over the PCI bus. Front panel mounted LEDs indicate various network activities.

The TPMC884-10 provides 10/100/1000 Mbit/s network connection via two front panel RJ45 connectors. The ports are galvanically isolated from the Ethernet Controller.

The operating temperature range is 0°C to +55°C.

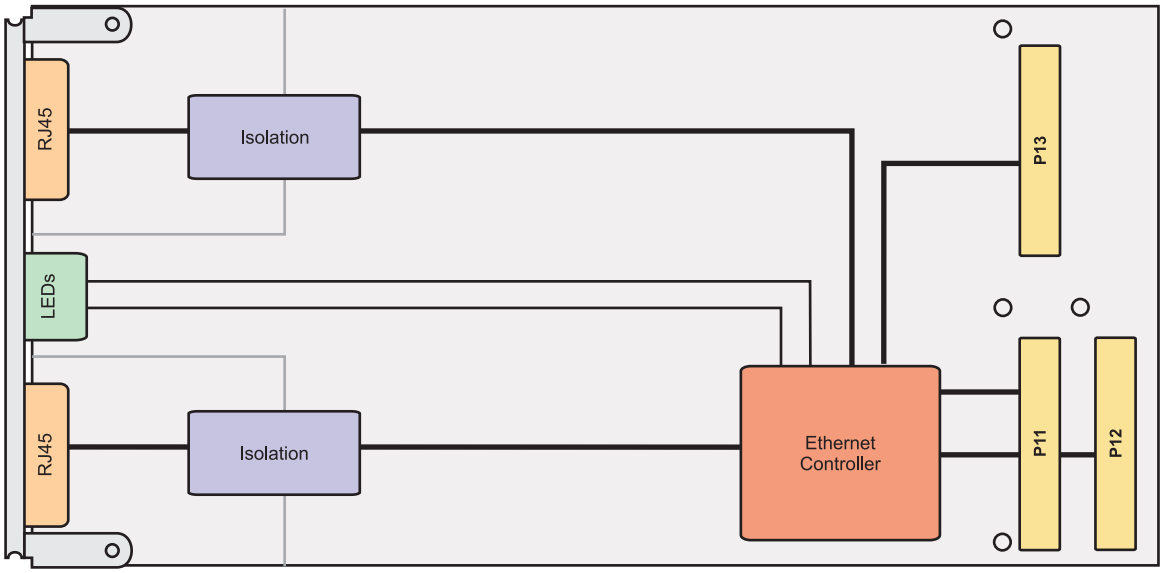

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI 2.2 (64 bit / 66 MHZ) and PCI-X 1.0a (64 bit / 133 MHz) compliant interface 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
Ethernet Controller with Integrated PCI and Physical Interface	Intel 82546EB	
Ethernet Interface		
Number of Channels	2	
FIFO	64 Kbyte Transmit and Receive FIFOs for each Channel	
Interrupts	Using PCI INTA and INTB	
I/O Connector	2 x Front panel Modular Jack	
Physical Data		
Power Requirements	1500 mA typical @ +3.3V DC	
Temperature Range	Operating Storage	0°C to 55°C -40°C to +70°C
MTBF	346000 h	
Humidity	5 – 95 % non-condensing	
Weight	75 g	

Table 2-1 : Technical Specification

3 82546 Gigabit Ethernet Controller

3.1 82546 PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x1010_8086
0x04	Status		Command		0x0230_0007
0x08	Class Code			Revision ID	0x0200_00xx
0x0C	BIST	Header	Latency	Cache Line	0x0000_xx00
0x10	PCI Base Address 0 (Memory Mapped Configuration Register)				0xFFFE_0000 (128 Kbyte)
0x14	PCI Base Address 2 (Memory Mapped FLASH Space)				0xFFFF_0000 (64 Kbyte)
0x18	PCI Base Address 1 (I/O Mapped Configuration Register)				0xFFFF_FFF9 (8 Byte)
0x1C	Reserved				0x0000_0000
0x20	Reserved				0x0000_0000
0x24	Reserved				0x0000_0000
0x28	Reserved				0x0000_0000
0x2C	Subsystem ID		Subsystem Vendor ID		0x0374_1498
0x30	Expansion ROM PCI Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_00DC
0x38	Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0x00FF_0100
0xDC	Power Management Cap.		Next Cap.	Cap. ID	0x7E22_0001
0xE0	Reserved	Data	Power Management CSR		0x4B00_4000

Table 3-1 : 82546 PCI Header

3.2 Configuration EEPROM

After power-on or PCI reset the 82546 loads the initial configuration register data from the on board configuration EEPROM.

See the 82546 Manual for more information.

EEPROM Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0xYYYY	0xYYYY	0xYYYY	0x0420	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x10	0x0000	0x0000	0x4406	0x0374	0x1498	0x0374	0x1498	0x30E8
0x20	0x0000	0x0374	0x0000	0x0000	0x38C8	0xFFFF	0xFFFF	0xFFFF
0x30	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x40	0x0000	0x7863	0x0000	0x0000	0x28C8	0xFFFF	0xFFFF	0xFFFF
0x50	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0x0602
0x60	0x90EC	0x0000	0x0000	0x0001	0x90EC	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0xZZZZ

Table 3-2 : 82546 Configuration EEPROM Settings

YYYY = Individual Ethernet Address Channel A. If the Ethernet address for Channel A is even, then Channel B is the Ethernet address for Channel A+1. Otherwise, the Ethernet address for Channel B is Channel A-1.

ZZZZ = EEPROM Checksum

4 Pin Assignment – I/O Connector

4.1 Front Panel I/O Connector

Pin	Signal
1	TX0/RX0+
2	TX0/RX0-
3	TX1/RX1+
4	TX2/RX2+
5	TX2/RX2-
6	TX1/RX1-
7	TX3/RX3+
8	TX3/RX3-

Table 4-1 : Per Channel Front I/O Pin Assignment

4.2 Front Panel LED Indicators

Each Ethernet Channel provides 4 LED indicators: 100, 1000, LINK and ACT. See table below for detail:

Name	Description
100	Indicates 100BaseT Speed when LED is on
1000	Indicates 1000BaseT Speed when LED is on
LINK	Indicates Link established when Led is on
ACT	Indicates Activity when LED is on

Table 4-2 : LED Status Definitions

When both Speed LEDs are off, then a 10BaseT Speed connection is established.